Design of FPGA-Based Data Acquisition System for the Interferometer

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Abstract

In compliance with the characteristics of the reference interference system in the Fourier transform infrared spectrometer, the paper puts forward a FPGA-based data acquisition system for the signal sampling of laser interference. This system adopts SRAM as the memory and the serial port transmission technology. Under control of FPGA, data of the interference signal are successfully acquired, stored and transmitted with finite state machine as the timing control mode. The acquired interference signal of laser shows that the data acquisition system is effective.

Keywords: Field Programmable Gate Array (FPGA), data acquisition, laser, module

1. Introduction

The laser interferometer is the reference interference system of the Fourier transform infrared spectrometer. When the moving mirror of the Fourier transform infrared spectrometer is in uniform motion, the laser, with a wavelength of 632.8nm, works together with the target infrared radiation to modulate the main interference system of the spectrometer. To meet the requirements of the equal optical path difference sampling in the spectrometer, we need to acquire the real-time signal of the laser interference, which is then used as a trigger control signal in the equal optical path difference sampling.

Traditional data acquisition systems are characterized by Micro Control Unit (MCU) or Digital Signal Processor (DSP) as their core control units, whose functions are mainly realized by the way of software running. However, in space applications, due to the intensive electromagnetic interference or other incidental factors, the odds are that MCU or DSP may have overstepped the normal program flow and run away, decreasing the reliability of the data acquisition system (Zheng, Liu, Zhang, Zhuang, & Yuan, 2014; Wang, 2010).

In the application of space remote sensing, the Field Programmable Gate Array (FPGA) devices have evolved to maturity with fine safety and high reliability. Its high reliability is manifest by the fact that the whole system can be put into the same chip, which is easy to manage and shield. Additionally, the flexibility of FPGA hardware structure makes it a good candidate for real-time processing of large capacity data, because its programming characteristics fit well in with the modularization design like those of programmable logic devices (Laird, Szymanski, Ryan, & Gonzalez-Alvarez, 2013; Chen, Qiao, & Gu, 2009). Based on FPGA chip APA300, this paper proposes a design method of the interferometer data acquisition system. In this design, the system control core APA300 has high stability and embodies the performance of Application Specific Integrated Circuit (ASIC) and the flexibility of FPGA, making it a good choice for the application of space remote sensing instruments.

2. Architecture of the Data Acquisition System

In the data acquisition system, all logic control is realized by hardware programming, which lowers the complexity of peripheral circuits, and simplifies the circuit structure. Thus, the size of the circuit can be considerably reduced and the circuit speed is then enhanced, making it possible for the construction of an online programmable data acquisition system (Liu, & Wang, 2011; Xin, Li, Hua, Song, Di, & Zhou, 2012). After

collimation and beam expansion, He-Ne laser signal passes through the silicon photoelectric detector whose output signal is a weak electrical signal with noise. This signal is directly converted into voltage signal by the conditioning circuit, and then converted from the analog signal to the digital signal by the A/D conversion circuit. Finally, the digital signal is processed and the output is the interferogram. The workflow of the laser interferometer data acquisition system is shown in Figure 1.
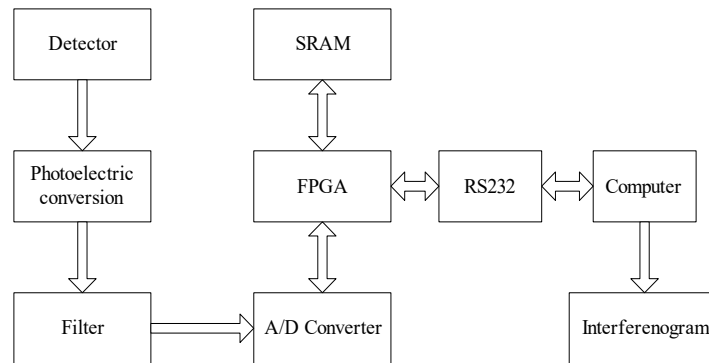

Figure 1. The block diagram of the data acquisition system

As the control unit of this system, FPGA is responsible for functions of signal processing, logic arbitration and timing management. Meanwhile, FPGA also provides clock signal for A/D conversion, and generates timing for the control A/D sampling, and the reading and writing of SRAM. The data acquisition system converts the analog signal output from the detector to digital signal, and then transmits the digital signal to FPGA.

3. Design of Peripheral Circuits

To achieve the above analog-to-digital conversion for the filter output, the data acquisition system of the interferometer should single out an appropriate A/D converter for the A/D converting circuit. The maxim sampling rate of THS1401 is 1MSPS, and 3.3V single power supply should be provided for the built-in sample-and-hold circuit and the reference voltage source. In addition, the resolution of THS1401 is to reach 14 bits. Accordingly, by drawing on the SRAM data storing mechanism, this system is realized by the A/D converting circuit made up by the 14 bits parallel A/D converter THS1401. The circuit is presented in Figure 2.
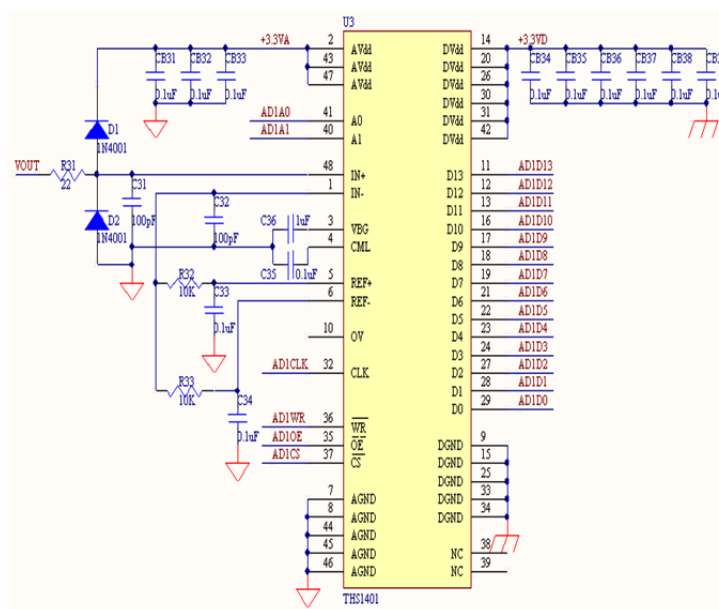

Figure 2. The A/D converting circuit

SRAM is a common data storing device. It can be connected to the A/D converter and the main controller by the three-state buffer gate respectively. When A/D converter is sampling, the SRAM is switched from the three-state

gate to the A/D converter, and the A/D converted data are written to SRAM. When the A/D sampling is finished, the data are read from the SRAM by the three-state gate switching to the main controller. The system selects the SRAM memory CY7C1021 to cache the digital signal of the laser interference from the acquisition module. The SRAM storing circuit is shown in Figure 3.
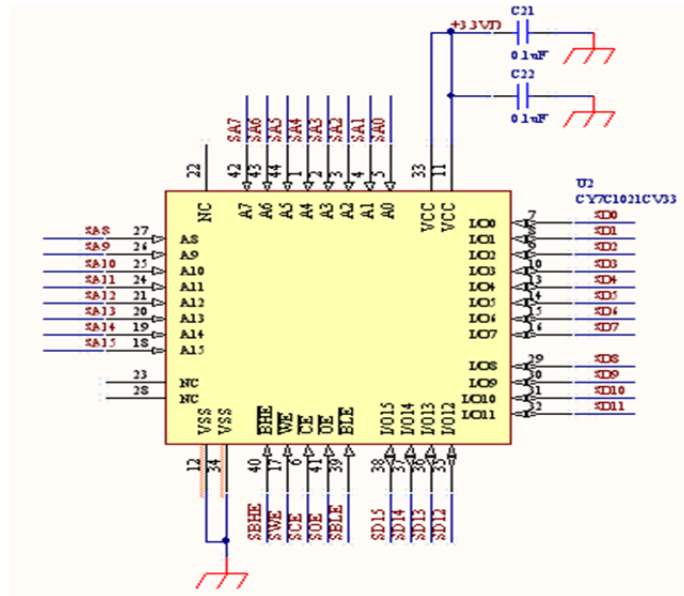

Figure 3. The SRAM storing circuit

The data stored in the SRAM are ultimately transmitted to the host computer through the RS232 interface. Since the serial interface of the computer terminal is the negative logic level of RS232, it is important to perform the level conversion. This system uses MAX3232 to achieve level matching. MAX3232 is a TTL level and RS232 level transform device with a 3.3V single power supply. It follows that four capacitors with $0.1\ \mu F$ will suffice to complete the level conversion between TTL and RS232. The circuit is shown in Figure 4.
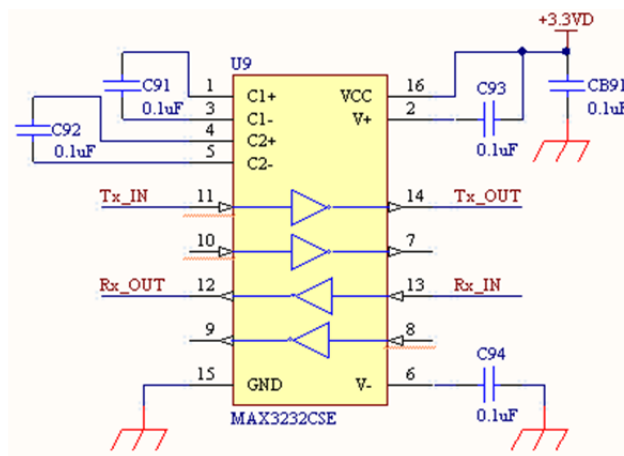

Figure 4. The serial port communication circuit

4. FPGA Control Unit

In the FPGA-based data acquisition system, the functions modulated by FPGA are divided into several independent modules. Each module function is realized by Verilog Hardware Description Language (HDL) programming, which makes peripheral circuits align and coordinately work under the control of the FPGA. As a result, the modularized design is implemented in the data acquisition system.

4.1 Serial Port Baud Rate Setting

The RS232 uses an asynchronous communication protocol, which means that there is not clock signal for the data transmission. However, the receiving port should, in some way, be synchronized with the receiving data. One way out is to set the serial port baud rate and the transmission format. The implementation can be broken into three steps. First, a serial baud rate is generated by the frequency divider in FPGA. Then a start bit and a stop bit are set for the serial port transmission respectively. Finally, the finite state machine is utilized to ensure the state transition of the serial transmission in consecutive order.

The serial baud rate can be set through the bus interface module. Each data width of the serial port is 8 bits at both the sending and receiving ports. With the start bit and the stop bit of serial data frame included, we have 10 bits for each data width for sending and receiving. In this paper, the serial baud rate is set at 9600, so the corresponding output clock frequency of the baud rate generator is 96 kHz. It should be noted that the system output clock of the FPGA Phase-Locked Loop (PLL) core is 12.8MHz. After different values are written to the register of the baud rate generator by bus, desired serial baud rate can be generated with a counter. Changes made to the counter value produce the desired baud rate (Zhai, Ji, Sun, & Xu, 2013).

4.2 Timing Logic Control

The timing control of the data acquisition system is accomplished by the Finite State Machine (FSM). The host computer executes the logic control on the FPGA chip APA300, while the FPGA receives instructions from the host computer and sends them to individual function modules. In this way, the data are acquired and uploaded to the host computer.

When the data acquisition system is running, the system is then initialized, which automatically sets the starting mode of the FPGA to the state waiting for instructions of the host computer. The output of PLL kernel is the global system clock, which subsequently generates the reset signal. Then the FSM is in a reset state. Upon the arrival of instructions, FPGA analyzes these instructions from the host computer. If the instruction is to start data acquisition and A/D sampling control signal has also arrived, then the A/D conversion commences, stimulating the FSM into the state of circulating acquisition. After the A/D conversion, 14 bits digital output of the A/D converter is written to the SRAM. When data in the SRAM reach 1024 kilobits, the A/D converter stops sampling. Afterwards, the data are read from the SRAM. These data are then transmitted to the host computer through the serial communication mode in real time.

5. Applications

Successfully applied to the laser interferometer, this system has realized data acquisition and transmitted the data to the host computer. With a He-Ne laser with a wavelength of 632.8nm, the interferometer can acquire the laser interference signal as is illustrated in Figure 5. Regarding the data acquisition, this interferometer system has displayed three prominent features: great precision, high speed and real-time transmission through the serial port to the host computer after each sampling.
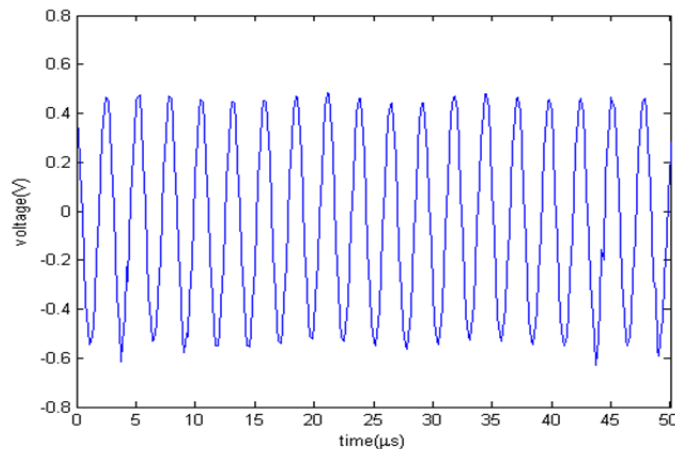

Figure 5. The laser interference signal

As can be seen from Figure 5, the laser interference signal is a sinusoidal signal with a smooth wave. It needs to be pointed out that the modulation frequency of the laser interference signal varies with the velocity of the interferometer moving mirror. Besides, there are also mediating factors like the laser power drift and the interference modulation depth. Taken these influences together, slight fluctuations are somewhat unavoidable in the amplitude of the laser interference signal (Yan, Chen, Sun, & Zhang, 2012).

6 Conclusions

By drawing on the characteristics of the reference interference system in the space Fourier transform infrared spectrometer, we have put forward a FPGA-based data acquisition system for the signal sampling of laser interference. With the assistance of the hardware description language Verilog HDL programming, we have successfully integrated data storage, output interface and other functional modules into the FPGA for further processing, so that the flexibility of the applicability of the system is greatly enhanced. The experimental results show that the laser interference signal obtained by the system is in perfect agreement with the theoretical analysis, verifying the feasibility of the design of the data acquisition system.

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