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Comprehensive Analysis of Auto Synchronization Techniques in Solar Photovoltaic Grid Connected Systems

K. N. Dineshbabu[1], R. Ramaprabha[2], V. Rajini[2], Kamal Bansal[1] & Bala Vinayagam[3]

[1] University of Petroleum & Energy Studies, Dehradun, India

[2] SSN College of Engineering, Kalavakkam, Tamilnadu, India

[3] Product Manager, GE Energy Management, Digital Energy, Canada

Correspondence: K. N. Dineshbabu, University of Petroleum & Energy Studies, Dehradun, India. Tel: 91-9790-920-721. E-mail: dineshbabukn@gmail.com

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Abstract

In this paper, an attempt to compare the performance of auto synchronization techniques such as zero cross detection technique, charge pump phase locked loop and synchronized reference frame phase locked loop has been made. The auto synchronization techniques are designed to reduce the mismatch between the grid voltage and inverter voltage parameters, which can further improve the delivered power quality thereby preventing grid islanding conditions. Such three different systems are analyzed using MatLab-Simulink and their performances are compared in compliance with IEEE 929 standards prescribed for power transfer from inverter to grid and IEC 61727 / IEEE 1547 standards for harmonic limitation of grid connected inverters.

Keywords: solar photovoltaic array, synchronization, charge pump phase locked loop, IEEE 929, IEC 61727, IEEE 1547, MatLab

1. Introduction

Increasing power demand requires the harnessing of renewable energy sources with conventional power generation methods. Due to the advantages and availability, the solar power generation becomes more attractive. Solar photovoltaic (SPV) systems produce direct electricity; hence they are popular in rural electrification as stand-alone system. Apart from this, nowadays there is a trend in using grid connected SPV system to meet growing power demand. Grid connected SPV system has several advantages as mentioned in literature (Mukerjee and Nivedita, 2011, p. 279-310). As SPV system generates dc, grid interactive inverters along with power conditioning unit (PCU) are normally used to interconnect with the grid (Dugan and Price, 2002). There are certain issues related to grid connected systems which should be properly addressed (Chris, 2009).

Frequency fluctuation is a common scenario in grid connected systems due to load variations and power swings. If the source is a generator, the frequency variation can be matched with suitable speed control techniques. But, in grid connected SPV system, due to the nonexistence of rotating equipments, the relationship between speed and frequency does not exist; thereby forcing an alternate method for control. The stability of the SPV grid connected system is further challenged by partial clouding issues. These issues would have a direct impact on all the frequency dependent functions like synchronization, load frequency control, active and reactive power control.

The challenges in synchronization involves magnitude, frequency and phase angle of the voltage at the point of common coupling (PCC) and SPV system has to be matched. Some of the techniques that are being used and proposed in literatures are as follows

- Zero cross detection technique (ZCD).
- Charge pump phase locked loop (CP-PLL) (Swanand)
- Synchronized reference frame phase locked loop (SRF-PLL) with moving average filter (MAF) (Dinesh)

Working principle and design of the above methods were dealt in detail in literature. The method of following the phase angle and frequency of the grid voltage after synchronization is called as an auto synchronization technique (Sahasrabudhe et al, 2005). Harmonics, load variations, system disturbance would affect the

performance of the above mentioned control techniques which is against the auto synchronization technique. IEEE 929 standard specifies the tolerance limits beyond which grid interactive inverters would be islanded and IEC 61727 and IEEE 1547 standard dictates the harmonic limits for 10 kW and 30 kW respectively (Sahasrabudhe et al, 2005).

In this paper, the above mentioned techniques have been tested subject to various scenarios that are likely to occur in a grid. The responses of these techniques are compared. The compliance of the results with IEEE 929, IEC 61727 and IEEE 1547 standards are also presented.

2. System Description

The block diagram of grid connected SPV system has been discussed in (Dinesh et al, 2011). In this system, the control circuit has been replaced by the aforementioned techniques as shown in Figure 1. Power quality, synchronization and reliability may interfere with the normal behaviour of the system if the issues mentioned in Section 1 are not addressed. The output of SPV system is fed to an inverter for grid integration and the inverter should be capable of adapting to the changes in the grid and PV system without compromise on its performance for disturbances in the grid.

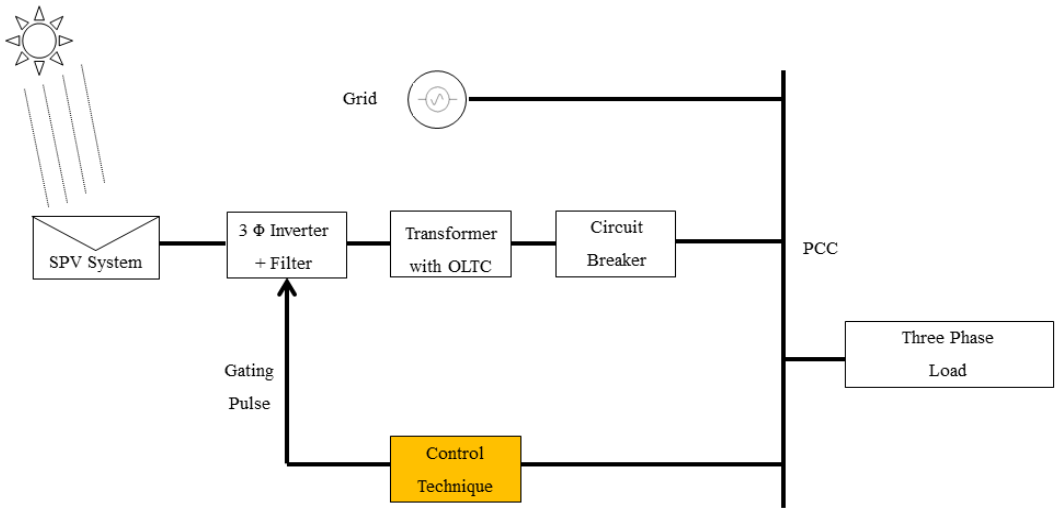

Figure 1. SPV Grid Integrated System with generalised control technique

Figure 2 shows the schematic diagram of the system that would be used to test the aforesaid techniques against the standards for scenarios mentioned in Section 3.

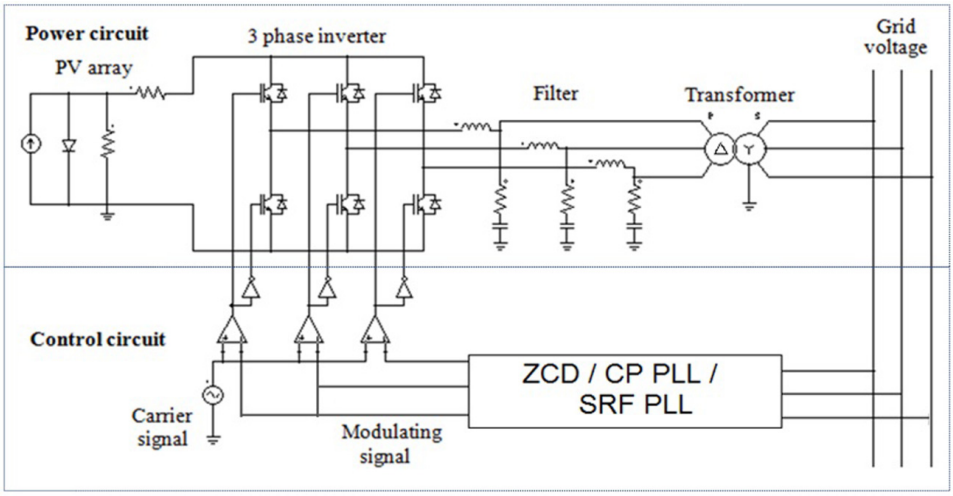

Figure 2. Schematic diagram of the system under test

SPV system feeds the grid with a control technique to maintain synchronization. Inverter firing is based on the comparison of modulating signal and carrier signal (Muhammad, 2004). The pulse width modulation (PWM)

depends on the quality of the modulating signal. The reference voltage is taken from the PCC. The PWM pulses are generated based on modulating signal and different control techniques are tested with scenarios that occur during grid disturbance.

The grid voltage is assumed as a balanced three phase symmetrical voltage source during the design of ZCD, CP-PLL and SRF-PLL techniques (Dinesh et al, 2013). The reference voltage is fed along with odd and even harmonics and the response of the system is analyzed in the following sections.

The parameters of the PV system (where single PV panel consists of 36 cells in series) used in this work are:

Grid voltage	:	415 V
PV panel voltage	:	16.54 V
PV panel current	:	2.25 A
PV Array size	:	14x2 (14 panels in series and 2 panels inparallel)
PV array voltage	:	230 V
PV array current	:	4.5 A
Frequency	:	50 Hz

In Figure 2, dc output from the SPV system is converted to ac by using a three phase inverter with a suitable PWM technique. The inverter output is fed to a filter to eliminate harmonics and the output is fed to a transformer with on load tab changer (OLTC) mechanism. ANSI C84.1 standard states that the PCU voltage should be greater than the grid voltage for the system to deliver active power to the grid. This is taken care by the OLTC transformer. A delta star transformer is used in this work since the 3rd harmonic would circulate in the delta winding and it would not be fed to the grid.

Table 1 summarizes the standards for grid connected SPV system which are used to verify the compliance of the results in this paper

Table 1. SPV system grid interconnection standards

Voltage Parameters	Standard
Magnitude	ANSI C84.1
Frequency	IEEE 929
Phase Angle	IEEE 929
Synchronization	ANSI 25
Harmonics	IEC 61727, IEEE 1547

A synchronization check relay complied with ANSI 25 standard to verify the magnitude, phase angle and frequency of the voltage at PCC and PCU is used in this work.

3. Response of the System for Grid Disturbance

This section discusses the commonly occurring scenario in power system during a disturbance in the grid. A load variation in the grid is a common scenario which is simulated by changing the frequency of the voltage at PCC. Harmonics in grid are also common and various harmonics are introduced at PCC to verify the harmonic content at load current.

FFT analysis is done at every stage to find the total harmonic distortion (THD) of the system. Figure 3 and Figure 4 show the voltage spectrum at PCC and its FFT (Fast Fourier Transform) respectively. Figure 5 and Figure 6 show the inverter current spectrum and it's FFT for ZCD technique. Figure 7 and Figure 8 show the corresponding response of CP-PLL technique. Figure 9 shows the harmonics rich input voltage spectrum (up to 33rd order) given for SRF-PLL. The FFT of the same is shown in Figure 10. The harmonic content of the output current spectrum with SRF-PLL is shown in Figure 11.

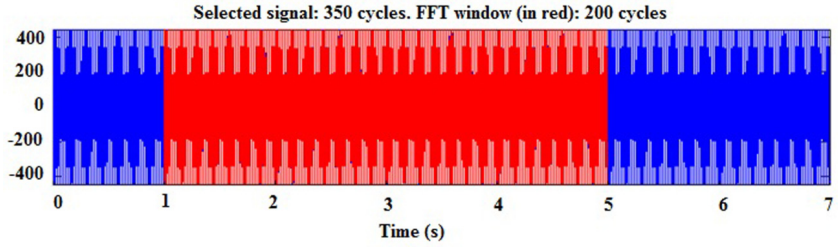

Figure 3. Voltage spectrum at PCC

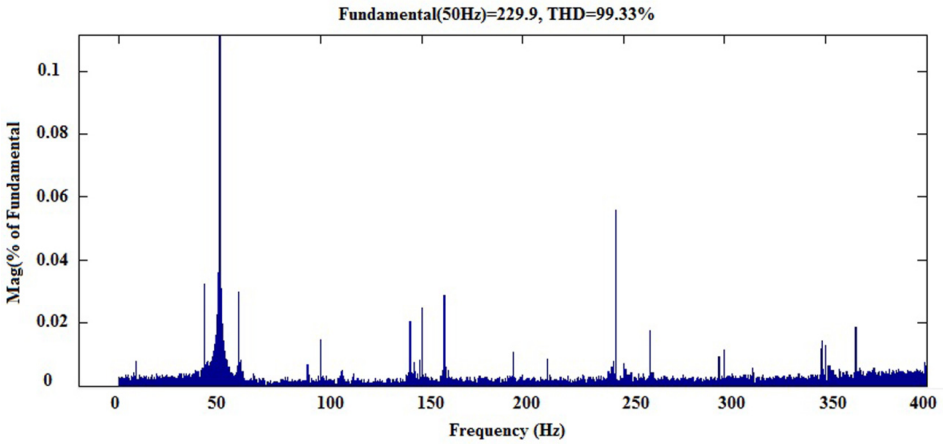

Figure 4. THD of voltage at PCC

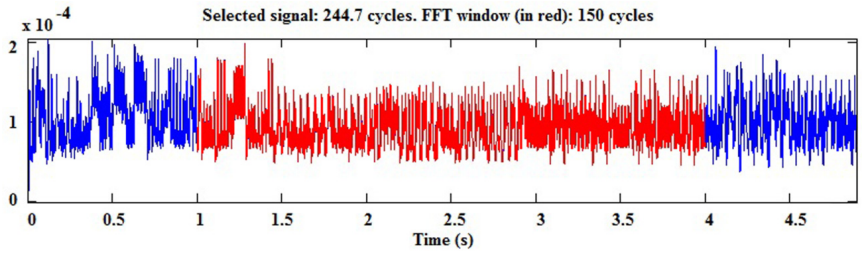

Figure 5. Current spectrum at PCU in ZCD technique

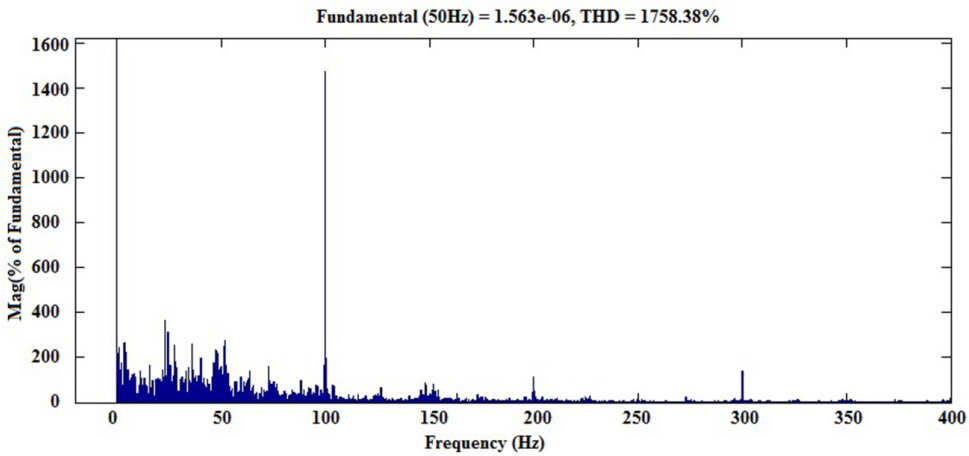

Figure 6. THD measured at PSU in ZCD technique

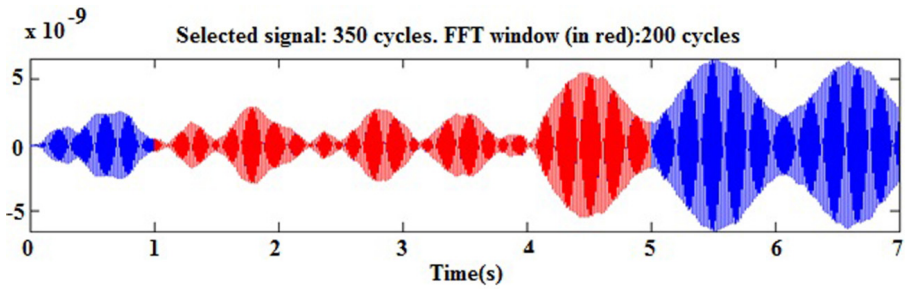

Figure 7. Current spectrum at PCU in CP-PLL technique

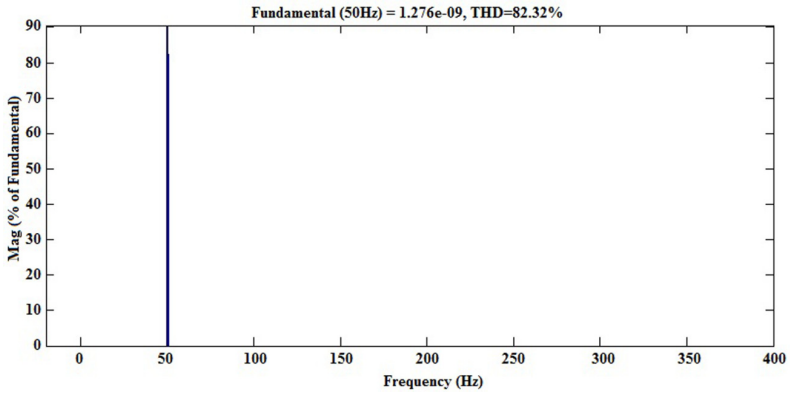

Figure 8. THD measured at PCU in CPPLL technique

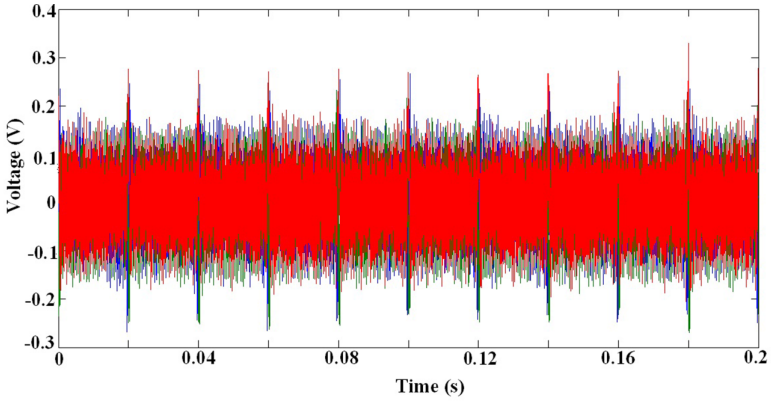

Figure 9. Harmonic rich input voltage spectrum for SRF-PLL

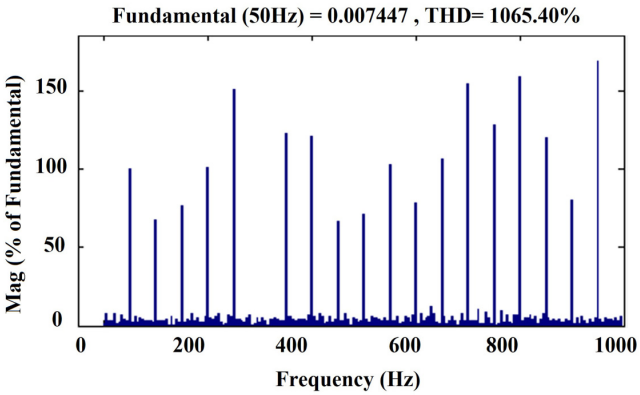

Figure 10. FFT of the harmonic rich input voltage spectrum for SRF-PLL

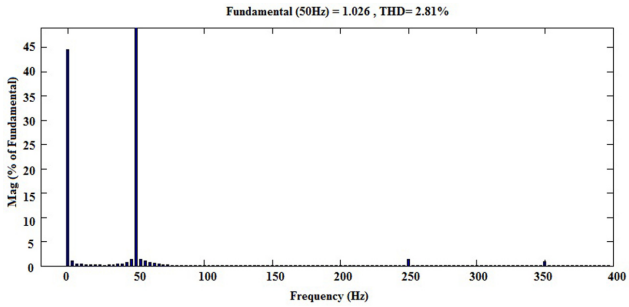

Figure 11. FFT of inverter current for SRF-PLL with MAF

To identify the harmonic suppression capability of the three techniques (ZCD, CP-PLL and SRF-PLL), the harmonics at the PCC was introduced as 5 % (with only 2nd, 3rd and 4th order harmonics). The analysis of the current spectrum at the output shows that the THD is 204.98 % in case of ZCD technique, 81.33 % in case of CP-PLL technique, but only 2.35 % in the case of SRF-PLL. Further the harmonics at the PCC was increased to 99.34 % (with only 2nd, 3rd and 4th order harmonics). The THD is found as 1758.38 % in case of ZCD technique, 82.32 % in case of CP-PLL technique, but only 2.75 % in the case of SRF-PLL technique. The spectrums for different techniques are shown vide Fig 5 to Fig 10. As per IEC 61727 and IEEE 1547 standard, the permitted value is 5 % THD. Excluding SRF-PLL, the other techniques yielded the results which do not comply with standards.

To check the effective operation of SRF-PLL with MAF technique further, the harmonic number is increased up to 33. Harmonic distortion to the tune of 1065.4 % in the voltage was introduced at the PCC to verify the ability of SRF-PLL technique. Even though, the harmonic of such high percentage are practically not applicable, to hi-light the capability of SRF-PLL technique, to address the worst case of harmonics, the test was carried out. The following observations have been made from Figure 6 to Figure 11. The harmonics at the output had a THD of 2.81 % in SRF-PLL with MAF technique. It was observed that the system with SRF-PLL and MAF complied with the above mentioned standard. When the test was repeated with ZCD and CP-PLL technique, the THD was observed to be extremely high and is displayed as infinity, that is, these techniques are not capable to address this kind of worst case.

From Figure 8 and Figure 11 we can conclude that SRF-PLL with MAF technique has dc components which are not available in CP-PLL. The presence of the dc component has increased the THD to 2.81 % which is still within the acceptable limits mentioned in the harmonic limitation standards. Though the dc component issue is a critical issue to be considered in grid connected system, it can be ignored as the solution is addressed in IEEE 929 standard. IEEE 929 standard states “Inverter manufacturers generally use one of two methods to prevent the injection of dc current into the utility interface. One method is to incorporate an ac output isolation transformer in the inverter. The other method, which uses a shunt or dc-current sensor, initiates inverter shutdown when the dc component of the current exceeds the specified threshold”. Implementation of these methods would nullify the dc components and thus the THD would further reduce from 2.81 %. Table 2 shows the consolidation of the results.

Table 2. Current harmonics distortion of different methods for different scenarios

IEC 61727 / IEEE 1547 Standard Compliance (THD < 5 %)				
Scenario	Injected harmonics (%)	THD (%)		
		ZCD	CP-PLL	SRF-PLL
Practical	5	204.98	81.33	2.35
Maximum measurable	99.33	1758.38	82.32	2.75
Worst case	1065.4	Extremely high	Extremely high	2.81

4. Results and Discussion

Load variation is another common scenario in grid connected system which will be accompanied by system unbalance and power swing. Power system faults will also result in load throw where dc transients and harmonics would be available during the sub transient and transient period. ZCD and CP-PLL method have failed for harmonic conditions as explained in Section IV. Voltage phase angle mismatch between the PCC and PCU is addressed in CP-PLL method; however CP-PLL method cannot distinguish load variation and harmonics. This defeats the advantages of CP-PLL since the system goes out of synchronization violating IEEE 929 standard. The inferences from this work are listed in Table 3.

Table 3. Test Results summary

	Capability of methods to meet Grid Scenario for the standards	
Methods	Harmonics	Sudden disturbance
	IEC 61727 / IEEE 1547	IEEE 929
ZCD	Fail	Fail
CP-PLL	Fail	Pass
SRF-PLL	Pass	Pass

5. Conclusion

In this paper, a detailed analysis of the harmonic issues in grid synchronization techniques has been discussed. The modulating signal for inverter is taken from the PCC. The presence of harmonics in the grid affects the quality of the inverter output. The ability of the three different techniques to address this issue has been tested and the results are compared with standards. From the test results, it is inferred that the SRF-PLL method supersedes other techniques and is best suited for SPV fed grid connected systems.

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