

The Implement of MPEG-4 Video Encoding Based on NiosII Embedded Platform

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Abstract

Using software code to achieve video coding, reduce the cost and increase portability, present a scheme using Altera SOPC to control data coding for MPEG-4 video software compressing system. According to use the DE2 board of Altera, implementing coding image data's input and output through the USB port on the board, achieves the input image MPEG-4 encoding using the configural NiosII embedded soft processor. Aiming at MPEG-4 video compression, the design adopts dynamic sprite encode to code the image data efficiently.

Keywords: MPEG-4, Sprite encode, SOPC NiosII, Embedded processor

1. Introduction

MPEG-4 ISO was formally announced in 1999 as an international standard by the Moving Picture Experts Group (ISO/IEC 14496, 1999). MPEG-4 and MPEG-1 and MPEG-2 are very different, and its compression ratio is greater, and it is the target encoding. MPEG-4 not only has a body compression algorithm, it is an international standards of integration and the demand for compression technology such as a digital television, interactive graphics applications (synthetic audio-visual content), interactive multimedia (WWW, information intake and decentralized). It can meet the needs of the three ethnic groups - multi-media content creators, network service providers and end-consumers. In addition to the traditional MPEG-4 encoding and decoding of digital video features, it has a lot of compelling features, including object-based video content object access to the scene content-based scalability, video depository check, error correction capability. MPEG-4 compression standard can be achieved between the compressed frame. The average compression ratio up to 50:1 or even higher up to 100:1, a relatively high compression ratio, and have a unified format, a good compatibility (John Viega, 2002).

Systems using Altera's DE2 development board, using SOPC configurable soft-core embedded processor NiosII realizes MPEG-4 video standard. Through the hardware design and software programming will be a large number of control and access to a wide range of peripherals to a rational allocation of work to meet the timing and functional requirements. On this basis the compiler run the MPEG-4 video encoding process to encode QCIF video file. The implement of MPEG-4 Video encoding apply to the user's specific requirements and the reduction of the actual situation, which has flexibility, taking up less resources, the use of a wide range of highly specialized nature.

2. System structure and working principle

Systems encode streaming media file which can be CIF and QCIF format. System can be divided into two parts such as hardware and software and take full advantage of the advantages of NiosII processor.

Hardware realization of some of the major functions: system design is achieved by the FPGA-based Nios II, which is constituted mainly by operation, control, input and output interfaces and peripherals. (1) Operation part use NiosII 32-bit RISC embedded system design for the system clock frequency 50MHz. (2) Control in part is constituted by the real-time control and status display. (3) Input-output interface is achieved by the USB interface based ISP1362

controller. The use of the main mode, read from the USB peripheral processor to carry out cross-source codec, and the output file is transmitted by the USB to peripheral for preservation. (4) Peripherals can be extended, for example, U disk, PC camera, video player and so on. Select the specific application according to the practice.

Software realization of some of the major functions: Using the C language to realize MPEG-4 video coding. Read code files (format YUV4: 2:0) directly from the FLASH, for each frame image of the Sprite has been the overall image motion estimation and motion compensation, the encoding of the data after a deposit to the SDRAM. After encoding the holistic files, encoding the data to write FLASH one-time from SDRAM. In the system, encoding each frame takes about 0.481s. By test, if the algorithm running on the clock frequency of 2.8GHz Pentium 4 processor, time for each frame encoding is 7.48ms,and the rate can be as high as 133.69pfs.

3. Hardware design

Using SOPC Builder system development tool to create 32-bit Nios CPU, and using automated Avalon switch fabric to form the total line to connect the system together with peripheral equipment. Hardware acceleration units and commands of the definition of the word constitute a powerful 32-bit embedded processor system (as shown in Figure 1).

USB on DE2 board Philips use ISP1362 controller chip, which is the composition of an OTG controller, a host controller and a peripheral controller. They connected with each other through a data bus interface and an external processor. The chip of ISP1362 integrate OTG transceiver, a charge VBUS actuators, as well as pull and pull-down resistors, which is used to reduce the number of external components for reducing costs.

SOPC Builder configuration shown in Figure 2.

4. Software Design

4.1 MPEG-4 encoding

At present, MPEG-4 standard-based application programs are for the most hardware, but the use of a dedicated MPEG-4 encoder chip is difficult to achieve the upgrading and because of the high cost, poor flexibility. In the system, using software to achieve the MPEG-4 video coding. First of all, the video encoder to set encoding parameters, such as the VOP size, frame rate, coding format, coding parameters such as scan mode. And then read from the FLASH file data stream QCIF to encode based on the set of encoding parameters. And then writing encoded data streams based on the appropriate file format (MP4U) into the SDRAM memory. Aim at the MPEG-4 video encoding in several key areas described as follows:

1) Definition of VOP generation.

MPEG-4 encoding unit is the VOP, VOP generation is achieved through the video segmentation, video segmentation is to achieve object-based video coding system. Image segmentation technique based on the use of segmentation information, is divided into partitions based on the texture segmentation, motion-based segmentation and space-time segmentation. Coding based on the requirements for image segmentation is not very high, mainly due to the real-time, where a selection of the joint space-time automatic video object segmentation algorithm. The first time-domain algorithm based on the F-partition hypothesis testing approach to be the initial change detection template, and then through the morphology-based segmentation of the airspace to get the ultimate fusion of moving objects. This relatively simple algorithm that can better the prospects of moving objects will be separated from the background.

2) Dynamic sprite coding.

Sprite coding is a new generation of coding technology, which generated global motion estimation using video images Sprite background paragraph, and then code the Sprite image, the context of the subsequent frames are encoded relative to the frame of the motion parameters Sprite image coding. Based on the background of the smooth and texture characteristics of a great relevance for Sprite coding panorama use a direct space prediction method.

Dynamic Sprite coding as shown in Figure 3.Video sequence of the first frame use I-VOP encoding method, and the first frame of the reconstructed image in the encoding and decoding client side to establish the same initial Sprite image. The second frame use the overall motion estimation algorithm to estimate a global campaign between the current VOP with the former VOP. Using the reference point describe the movement between the two VOP. Method using P-VOP texture code the second frame which is different with the first frame in all the VOP macroblock such as the motion compensation mode in addition to the macroblock and block motion compensation, but also can be used as a reference for Sprite image motion compensation, when the macro motion compensation block for the global motion compensation. Decoder decoding the track to be the reference point for global motion parameters, and then decoding texture information is the second frame of the reconstructed image, according to global motion parameters and the second frame image reconstruction image update Sprite. The same method used for coding sequence behind the VOP.

4.2 USB host software process

The flow chart of the USB host software 4 below, the major software part including USB host and USB peripheral

function modules. They can be independent of each other while calling each other to jointly complete the USB host function. The entire process to complete disruption through scheduling to achieve the host function. When USB bus is in the work, the system is still in accordance with the specific running timing and protocol specification. If the system online through changed level in the data bus to detect USB devices connect in or out, and then host and peripherals on the basis of prior agreement of the order implement a series of information exchange.

To identify the host if it is a USB device must pass enumeration process, host use bus enumeration to identify and manage the necessary changes in equipment status. Bus enumeration process is as follows: (1) Equipment connect. USB device access to USB.

(2) Equipment power up. USB devices can use the USB bus-powered or an external power supply.

(3) Detected the host equipment reset signal. Equipment power up, the host device through the pull-up resistor to detect if a new device connects to the host port and sends a reset signal.

(4) Equipment by default. Equipment from bus to receive a reset signal, but cann't go on a bus in response to handling. Equipment reset signal is received, use the default address to addressing them.

(5) Address assignment. When the host device to receive the address of the default (00H) response time, distribution of equipment on a free address, equipment only can be response to the address.

(6) USB host read device descriptor to verify the properties of equipment.

(7) Device configuration. USB host device read the device descriptor to configure parameter, if the resources needed to meet the USB, transmit configuration commands to the USB device that means the end configuration.

(8) Hang. In order to save power, when the bus remain idle for more than 3ms, the device driver will enter the suspend state.

5. System Testing

In order to verify if the results of this coding is correct, we run the code on the PC-environment of VC++6.0 compiler to emluator running the same encoded video files, as well as the results will be decoded in VC++6.0. YUVViewer to show through the images before and after encoding: Figure 5 is the 13th frame image before encoding, Figure 6 is the frame image after decoding.

Comparison shows that MPEG-4 coding distortion is very small, NiosII now in order to verify the code is correct, as long as to compare the two results of each frame that are encoded on NiosII and VC++6.0. After encoding each frame comparison from the number of bytes. By the experimental comparison, their results are the same encoding. Finally, in the end the output encoding file on NiosII is decoded on PC, the results obtained in Figure 6. This can confirm that the coding in NiosII is entirely correct. Verify the file size before and after encoding, as shown in table 1.

Compression ratio mainly is relative to frame relevance in image, not the size of image files. According to statistics, it is available to get the average compression ratio of MPEG-4 that is the 50:1, higher to achieve more than 100:1.

6. Concluding remarks

Has been introduced an international compression standard MPEG-4 and a software code realization based on NiosII. Through the use of Altera's 32-bit embedded processor NiosII to develop software on QuartusII 5.1 IDE for the design of system. After experimental verification, embedded video coding system based on NiosII has the implementation of highly efficient compression and can achieve real-time requirements. System can be applied to monitor field, according the front terminal using USB camera without capture card, not only cost savings, but also be high stability, so the system has great value.

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Table	1	The	test	table	of MPF	-4 EG-4	com	nressing	rate
raute	1.	THC	iest	table	UT IVIT L		com	pressing	rate

Before encoding file	After encoding file	Compression	
Size (MB)	Size (KB)	ratio	
0.958	15.63	61.3	
3.486	53.49	64.8	
10.8	116	93.1	
72.5	1050	69.05	
72.5	1620	44.75	
76.1	335	227.2	



Figure 1. Main composing of system

101.661			Clock	Source	MHz	Pipeline	
Boar	d: Unspecified Board	•	clk	External	50.0		
			click to add.				
Devic	e family: <mark>Uyclone II 🔄 [</mark> Hardi	opy Conpatible					
Ike	Modula Nama		Description	<u></u>	[Innut Clock]	Rece	End IP
17		àñ Nice I Pro	cessor - Atere (Cornoration	clk	Dusc	
1V	instruction master	Mester nort	JUGSSUI - Millera V	Jurporaduri	UR I		
	data master	Master port				BOI	B0 31 6
	tag debug module	Slave port				0x01000000	0x010007EE
	- mag_actuag_notate	JTAG LART			ck	0x01004000	0x01004007
	⊞ sdram 0	SDRAM Con	roler		ck	0x00000000	0x007EEEEE
7	Fitri state bridge 0	Avaion Trist	ate Bridge		ck	(())))))))	((((((())))))))))))))))))))))))))))))))
	avaion slave	Slave port			11111		
	ristate master	Master port					
7	⊕ cfi_flash_0	Flash Memor	y (Common Flash	Interface)		0x00800000	0x008FFFFF
7	timer_0	Interval timer			clk	0x00900000	0x0090001F
7		System ID Pe	ripheral		ck	0x00900020	0x00900027
7 1-	time uart_0	UART (RS-2	32 serial port)		ck	0x00900040	0x0090005F
7	timer_1	Interval timer			ck	0x00900060	0x0090007F 3
7	⊞ lcd_16207_0	Character L0	D (16x2, Optrex	16207)	ck	0x00900030	0x0090003F
7		PIO (Parallel	10)		clk	0x009000C0	0x009000CF
7	⊞ led_red	PIO (Parallel	10)		clk	0x009000D0	0x009000DF
7		PIO (Parallel	10)		ck	0x00900120	0x0090012F 5
7		PIO (Parallel	10)		ck	0x00900130	0x0090013F
✓		SEG7_LUT_6	3		ck	0x00900028	0x00900028
7 -	⊞ sram_0	SRAM_168it	s_512K		ck	0x00980000	0x009FFFFF
7	⊞ I2C_0	Open_I2C			clk	0x009000A0	0x009000BF
7	epcs_controller	EPCS Serial	Flash Controller		clk	0x00900800	0x00900FFF 7
7		Interface to I	Jser Logic		ck	0x00900080	0x0090008F 4
		VGA Contro	ller		ck	0x00A00000	0×00EEEEEE

Figure 2. SOPC Builder configuration







Figure 4. The flow chart of USB host software



Figure 5. Before encoding



Figure 6. After decoding