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Chopper Stabilized, Low-Power, Low-Noise, Front End Interface Circuit for Capacitive CMOS MEMS Sensor Applications

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Abstract

In this paper, a chopper stabilized fully differential CMOS pre-amplifier circuit is presented. The proposed circuit is designed for sub-atto Farad capacitive CMOS MEMS sensing applications. Chopper stabilization technique is employed to minimize flicker (1/f) noise and offsets in the circuit. The proposed circuit is designed using MIMOS 0.35 μm AMS CMOS 3.3 V technology and simulation results from Cadence Virtuoso Spectre circuit simulator show that the proposed circuit is able to detect capacitance changes ranging from 0.0375 aF to 37.5 fF, attain an input inferred noise of 0.9 nV/√Hz, gain of 18.1 dB at 3-dB frequency of 5.5 MHz with total power consumption of 0.33 mW.

Keywords: MEMS (Micro Electro Mechanical systems), CMOS (Complementary Metal Oxide Semiconductors), chopper stabilization, pre-amplifier, monolithic, read-out circuit

1. Introduction

CMOS MEMS devices are extensively used in medical, industrial, chemical, environmental, military, robotics, aerospace, and navigation and guidance systems. They are the key elements in various accelerometers, gyroscopes, chemical sensors, bio-medical sensors, pressure sensors, level detectors, humidity sensors, Micro actuators, Oil exploration systems, earthquake monitoring, vibration monitoring, smart phones and game controllers (Fang, 2006; Jianghua, Xuewen, & Bangxian, 2009; Patra & Bhattacharyya, 2009; Shiah, Rashtian, & Mirabbasi, 2010; Zhao, 2009). Different sensing techniques have been explored and developed to meet the ever-growing demand of MEMS based sensor systems. Available sensing techniques include optical sensing (Bollschweiler et al., 2009), piezoresistive sensing (Zimmermann et al., 2005), tunneling current and piezoelectric sensing (Patra & Bhattacharyya, 2009) and capacitive sensing (Fang, 2006; Hongzhi et al., 2011; Jianghua et al., 2009; Shiah et al., 2010; Wu, 2002). Among all, capacitive sensing technique is the most dominant and widely used because of its greater stability, low sensitivity to temperature, and compatibility with VLSI technology.

Continuous advance in CMOS MEMS device fabrication and microelectronics technologies in the past few decades has resulted in robust, precise, and high performance sensor systems and applications (Fang, 2006; Hongzhi et al., 2011). Further miniaturization of the systems has led to lower power consumption, smaller size, low cost and higher mobility. Monolithically integrating the electrical circuit with the CMOS MEMS device in a single piece of silicon substrate further permits reduction of losses, leakages and formation of parasitic capacitances (Fang, 2006; Menolfi & Qiuting, 1998; Wu, 2002), as well as making it suitable for mass production. Moreover, this reduces number of required bonding pads and external wiring. This significantly boosted the reliability of CMOS MEMS based sensor systems (Aziz, Mamun, Bhuiyan, & Bakar, 2013; Fang, 2006; Jianghua et al., 2009; Nebhen et al., 2011; Shiah et al., 2010).

At the same time, however, miniaturization and power scaling of CMOS MEMS device fabrication are resulting in pre-amplified sensor output signals to become small in magnitude, making them highly susceptible to various noises and hence poor Signal to Noise Ratio (SNR) outputs (Fang, 2006; Menolfi & Qiuting, 1998; Wu, 2002). To address the above mentioned shortcomings, many researches have been conducted to improve CMOS MEMS sensor system performances on two major areas, namely device improvement and circuitry enhancement. The

former focuses on improving the design and fabrication of the CMOS MEMS device structure to yield improved output signal magnitude with better SNR. This approach concentrates more on boosting the device design performance by employing advanced fabrication technologies, materials, tools, and optimized design enhancement techniques. The latter focuses on improving the resistance of the interface circuit to internal and external noises and disturbances. It deals with ways to boost the performance of the interface circuit architecture by noise suppressing and improving sensitivity (Enz & Temes, 1996). The interface circuit is responsible for signal conditioning and amplification of the sensor output signal. By carefully designing the interface circuit it is possible to better condition and limit the effects of various noise in the readouts (Kader, Rashid, Mamun, & Bhuiyan, 2012).

Previous works (Hu & Sawan, 2002; Jianghua et al., 2009; Menolfi & Qiuting, 1998; Shiah et al., 2010) showed that using only a single stage amplifier for the interface circuitry to achieve both low noise and low power requirements is a challenging task. Hence Fang (2006), Wu (2002) and Nielson & Bruun (2004) implemented a multi-stage amplification scheme to meet the requirements. Whilst having multi-stage made high gain attainable, input referred noise remains the main constraint as high gain also brings together high input referred noise figure (Fang, 2006; Shiah et al., 2010). Since the sensor output signal is often weak, the input stage of interface circuits determine the overall noise performance (Fang, 2006; Nielsen & Bruun, 2004). To attain a low noise figure, it will require careful tradeoffs among parameters such as linearity, gain, output voltage swing, input and output impedances, power dissipation and noise performance (Baker, 2010; Razavi, 2001; Sedra, 2004).

This paper hence focuses on the design of the input stage of the interface circuit and proposes a fully differential CMOS cascode amplifier with chopper stabilization scheme. It is ideal for CMOS MEMS structures with capacitive sensing schemes and limited sensing capacitance changes as low as sub-atto farad ranges. The following sections explain the design and simulation results of our proposed circuit.

2. Minimizing Electrical Noise in CMOS MEMS Capacitive Sensors

Electrical noises are the main source of noise affecting the performance of capacitive CMOS MEMS sensors (Fang, 2006; Wu, 2002). This noise mainly constitutes flicker, thermal and shot noises. Flicker and thermal noise are the dominant whereas shot noises are significantly small and usually ignored. Flicker noise is inversely related to the frequency of operation hence highly dominant at low frequencies while thermal noise is directly proportional to the absolute temperature and not related to the frequency of operation as shown in Equations 1 and 2, respectively (Razavi, 2001).

$$v_f^2(f) = \frac{k_f}{2\mu_n (c_{ox})^2 WLf} \tag{1}$$

$$v_t^2(f) = \frac{4\gamma kT}{\sqrt{2\mu_n c_{ox}(W/L)I_D}} \tag{2}$$

where v_f is flicker noise, v_t is thermal noise, k_f is the flicker noise coefficient, μ_n is carrier mobility, c_{ox} is the gate capacitance per unit area, W and L are the channel width and length of the MOSFET respectively, γ is the MOSFET thermal noise coefficient, k is the Boltzmann's constant, T is temperature in Kelvins, I_D is the bias current of the MOSFET, f is the frequency at which the circuit is operating.

The main cause of electrical noise and degradation in the performance of CMOS devices are the parasitic gate capacitances. These capacitances arise from the parallel plate capacitor created between the gate plate and the induced channel of the CMOS device and because of the overlapping regions of the gate with the drain and source with the gate. The gate to source and gate to drain capacitances can be computed as given in Equation 3 and 4 (Baker, 2010; Razavi, 2001; Sedra, 2004);

$$c_{gs} = \frac{2}{3} WLc_{ox} + WL_{ov}c_{ox} \tag{3}$$

$$c_{gd} = WL_{ov}c_{ox} \tag{4}$$

where, c_{gs} is gate to source capacitance, L_{ov} is the overlapping length and c_{gd} is gate to drain capacitance. These capacitances tend to play a major role when the frequency of operation is high. Wu (2002) showed that flicker noise is the dominant noise in CMOS MEMS devices. However by employing optimum capacitance matching method the width of the transistors used for the input of the sensing circuit can be optimized resulting in a

structure with highly minimized total noise effects (Fang, 2006; Hongzhi et al., 2011; Wu, 2002). The optimization equation is given in Equation 5.

$$c_{gs} + c_{gd} = c_{stotal} + c_p \tag{5}$$

where, c_{stotal} is the total sensing capacitance and c_p is the parasitic capacitance. Equation 5 shows that when the gate capacitances are made to match the sum of the sense and parasitic capacitance values from the sensor, then a minimum total noise level of the transistor will be attained. This equation can be used for many CMOS MEMS device readout circuit design and synthesis. Hence this noise optimization equation is used in designing the proposed cascode front-end amplifier in this work.

The proposed interface circuit follows fully differential capacitive sensing scheme which has the merits of better noise and distortion rejection capabilities (Hongzhi et al., 2011; Kang, 2010). The sensed signals from such structure can be computed using Equation 6 (Wu, 2002).

$$V_{sense} = \frac{4 \times \Delta C}{2C_o + C_p} V_m \tag{6}$$

where, V_{sense} is the sensed voltage signal, V_m is modulation voltage, ΔC is change in the sensing capacitance and C_o is the static sensing capacitance.

2.1 Chopper Stabilization

Chopper stabilization technique is implemented to further reduce flicker noise and offset imperfections of the designed cascode front-end amplifier. Chopper stabilization is a technique operating based on the principles of using modulation and demodulation techniques (Enz & Temes, 1996; Fang, 2006; Hu & Sawan, 2002; Nebhen et al., 2011; Nielsen & Bruun, 2004). The sensed input signal will be amplitude modulated to a higher frequency, chopping frequency, where there is less or no flicker noise. Then the transposed signal in the chopping frequency will be amplified by the amplifier. Following that the amplified signal will be demodulated back to the baseband while the noise and offsets are unaffected remaining at the odd harmonics of the chopping frequency.

Both time domain and frequency domain illustration of chopper stabilization is shown in Figure 1. The input signal in time domain is modulated to a higher frequency by a square wave carrier signal prior to amplification resulting in a chopped signal transposed to the odd harmonics of the carrier signal frequency. The amplified signal is then demodulated back to the baseband, leaving the flicker noise and offsets behind, by the same carrier signal and unveiling an amplified final output. Whereas in the frequency domain, the input voltage spectrum is folded to the old harmonics of the square wave spectrum and amplified. The amplified signal spectrum in the odd harmonics is then once more folded back to the baseband leaving the spectral images and flicker noises in the higher frequencies. These spectral images and flicker noises are removed by using a low pass filter with cutoff frequency of a little above the baseband frequency.

2.2 Modulation/Demodulation

The modulation and demodulation of the front-end amplifier is realized by employing a set of CMOS switches (Fang, 2006; Nebhen et al., 2011; Nielsen & Bruun, 2004). These CMOS switches are maneuvered by two clocks; $\emptyset$ and its inverse phase equivalent $\emptyset_1$. The switches are made to alternate the input signal to realize modulation and demodulation. Hence chopper realization and noise minimization can be attained by modulating and demodulating the input signal by the chopping frequency of these sets of switches.

As shown in Figure 2, four switches are required to achieve chopper realization. Therefore four identical NMOS switches are used for this modulation and demodulation purpose. Further, it has been shown that by using half sized drain to source connected dummy switches it is possible to significantly minimize the main sources of noise (dynamic offset noise and charge injections) arising from the switches (Fang, 2006; Nebhen et al., 2011; Nielsen & Bruun, 2004). Hence dummy switches with an inverse clock of the main switches in both sides of the main switches are included and employed in this work.

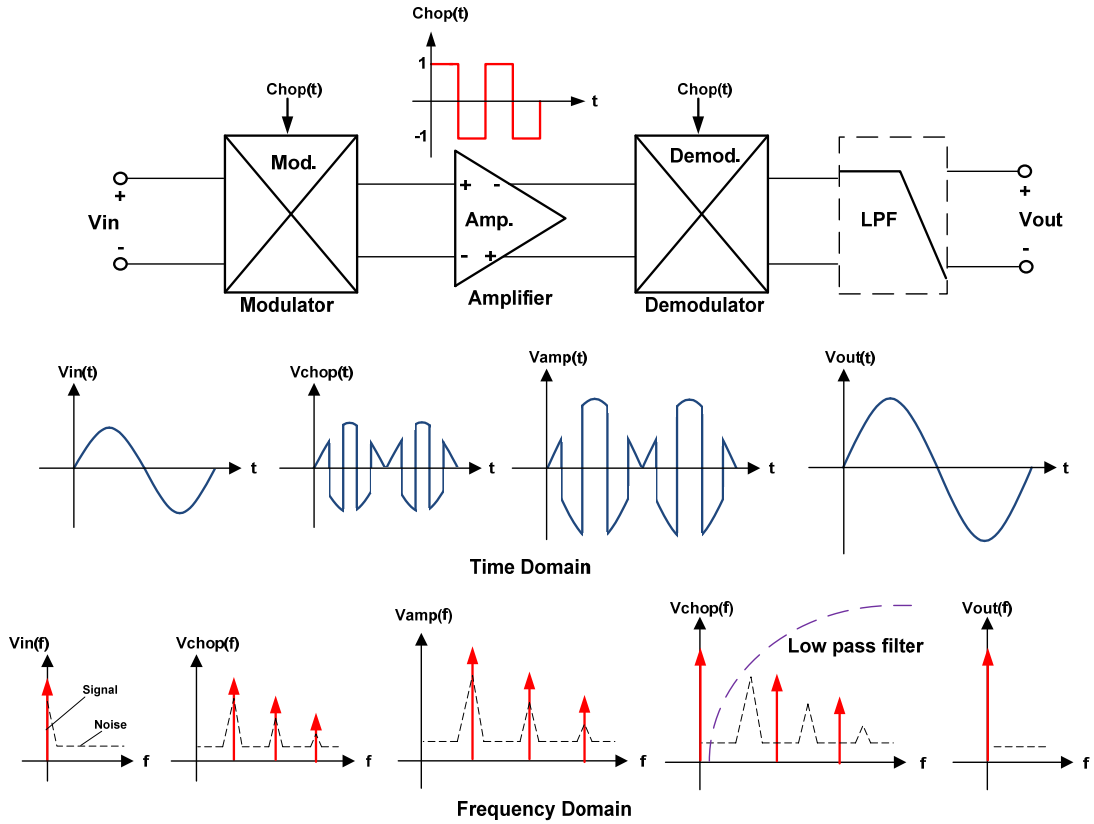


Figure 1. Chopper modulation principle

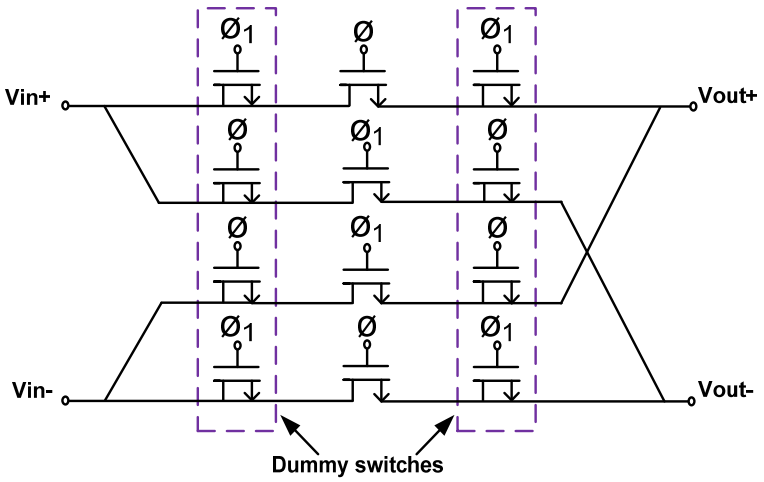


Figure 2. Transistor level implementation of modulator/demodulator

2.3 Proposed Low-Noise Cascode Amplifier

The proposed front end amplifier in this work is intended for applications in capacitive sensing interface circuit. Due to the sensing range (up to sub-atto farad), multistage amplification is usually required. Hence, in this work a front end CMOS cascode amplifier topology is presented for sensors requiring multi stage amplifications. Cascode amplifier has the advantage of achieving high input impedance and transconductance of the Common Source (CS) amplifier and the ability of attaining a super current buffering ability and a wider bandwidth of DC gain of the Common Gate (CG) amplifier (Baker, 2010; Razavi, 2001; Sedra, 2004). However, the main reason of choosing cascode amplifier lies on the fact that the very high input resistance of the CS amplifier and the low input resistance of the CG amplifier results in a structure which reduces the miller effect significantly and make

them preeminent in applications under high frequency operations.

Further, since CMOS amplifiers normally act like trans-conductance amplifiers by exhibiting large input and output resistances, it is necessary to combine them with trans-resistive loads or amplifiers to obtain decent voltage amplifiers (Allen & Holberg, 2002; Razavi, 2001). The schematic of the proposed circuit is given in Figure 3. The input transistors, M1 and M2, are made to be PMOS transistors to take advantage of their lower flicker noise coefficients compared to the NMOS equivalent. The length of the input MOSFETS are made to be twice the lowest possible in the process design technology ($L = 2 \times L_{min} = 0.7\mu m$) in order to reduce the effects of mismatches while keeping the parasitic minimum. These input MOSFETS alone form a Common Source amplifier structure and therefore M3 and M4 are connected to their drains to form a cascode amplifier. M3 and M4 are incorporated in the circuit for miller compensation and making the amplifier suitable for high frequency operation.

Among the different types of loads, current sink load is chosen for this work because of its quality of making the output gain linear and its ability of allowing larger output voltage swings (Razavi, 2001). Hence M5 and M6 shown in Figure 3 makeup the current sink loads. Furthermore, the aspect ratios of M5 and M6 are carefully tuned to meet the gain specification of interest. Meanwhile, since current supply is needed to drive the circuit, P-channel MOSFET current mirror supply is realized through M7. Appropriate biasing is supplied through Vb1, Vb2 and Vb3 from a separate biasing circuit. M7 is biased to operate in deep triode region and acts like a 100 μA current source. The circuit is made to operate under 3.3 V power supply.

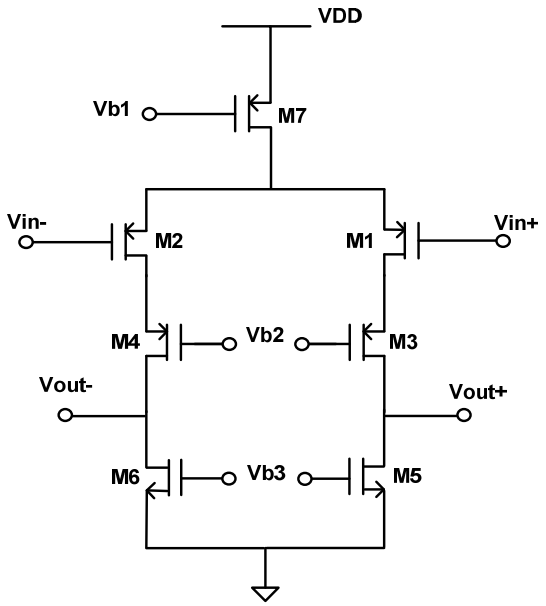


Figure 3. The cascode amplifier schematics

3. Simulation Result of the Proposed front End Pre-Amplifier

The low noise, chopper stabilized front end amplifier is simulated in Cadence Virtuoso Spectre circuit simulator based on MIMOS 0.35 μm AMS CMOS 3.3 V technology. Transient simulation of the modulator and demodulator design showed that the designed structure modulates an input signal to the chopping frequency of interest or demodulates it back to the baseband realizing chopper stabilization technique, as intended. Further simulation of the amplifier together with the chopper stabilization and 1 pF load capacitance showed that it attains a voltage gain of 18.1 dB. Figure 4 verifies the functionality of the chopper stabilization method designed and the overall amplifier for an input signal of 1 mV peak sinusoidal at 20 kHz frequency and chopping carrier square wave of 1 V peak at 1 MHz. Figure 5 shows the realization of the sub-atto to few femto farad capacitance change detection. It gives the response of the interface circuit for the minimum and maximum capacitance changes. The input voltage change of 10 nV in part (a) and 10 mV in part (b) with respect to the capacitance changes of 0.0375 aF and 37.5 fF capacitance changes respectively, based on Equation 6.

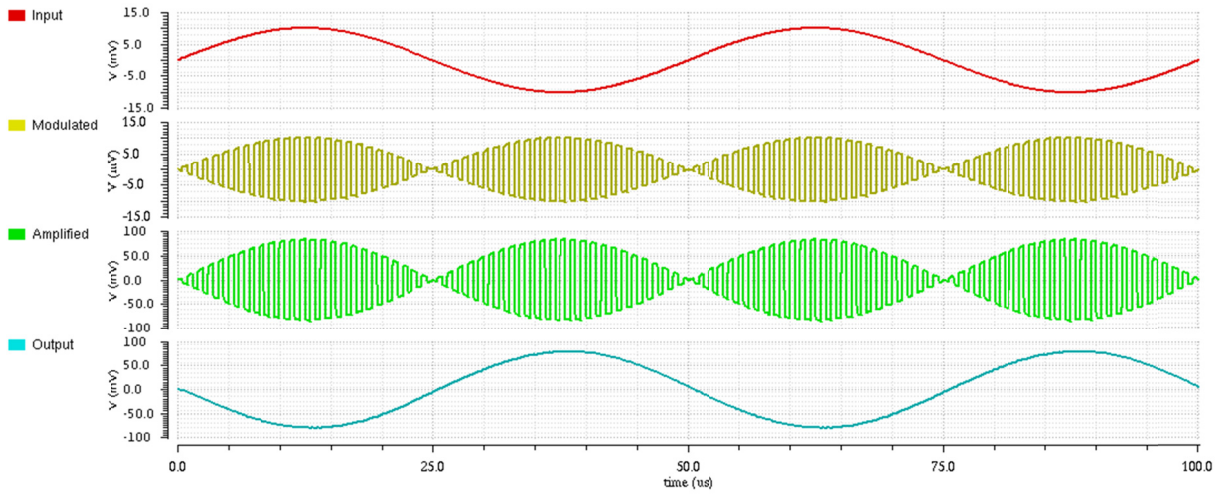
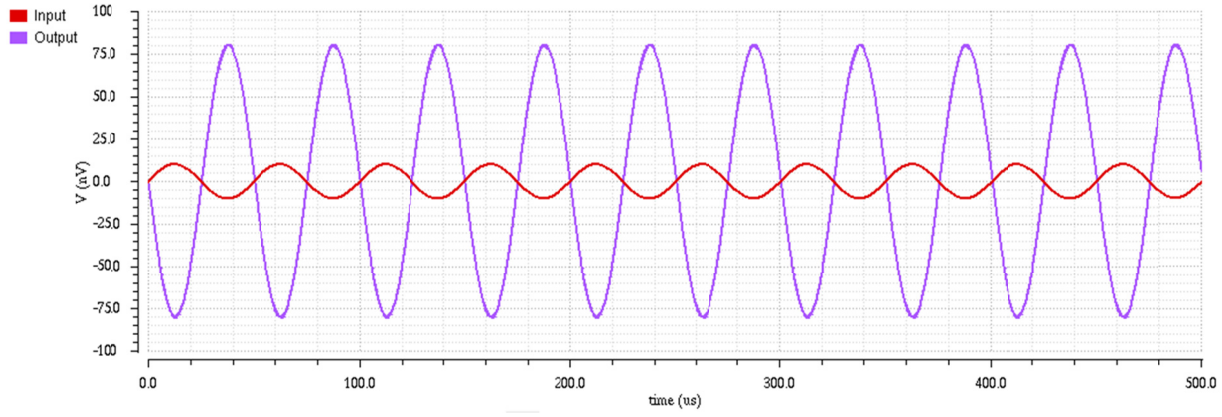
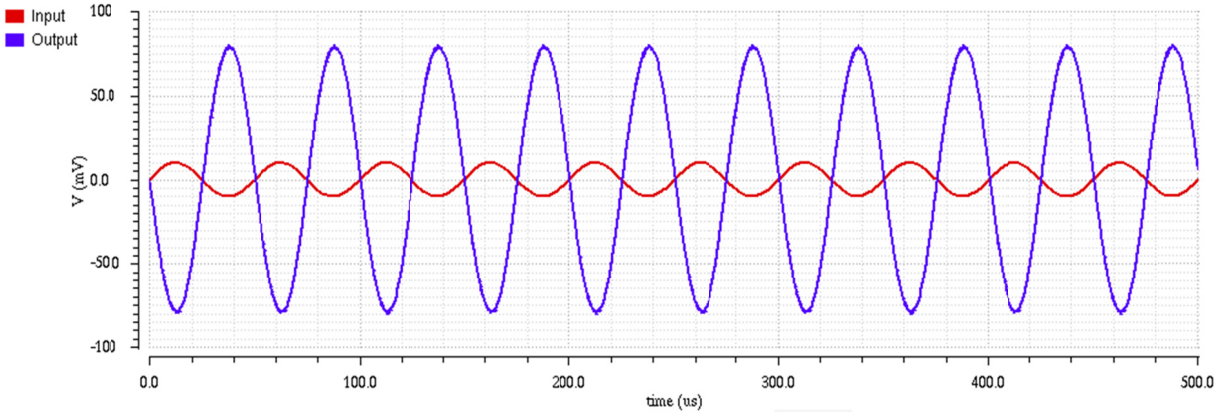


Figure 4. Transient analysis simulation result



(a)



(b)

Figure 5. Input and output relationship, (a) 0.0375 aF, (b) 3.75 fF

Figure 6 shows frequency domain gain simulation result indicating that the circuit attains a gain of 18.1 dB at a 3-dB frequency of 5.5 MHz, while Figure 7 shows the noise analysis indicating a total input inferred noise of the whole circuit to be 0.9 nV/ √ Hz. The interface circuit draws 100 μA current from a 3.3 V power supply implying total power consumption is 0.33 mW.

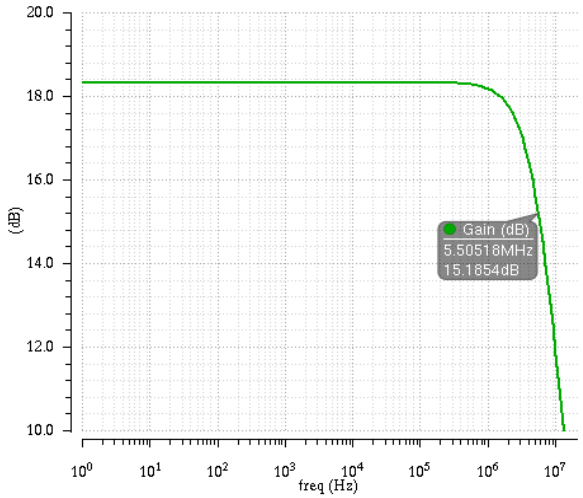


Figure 6. Frequency domain gain simulation result

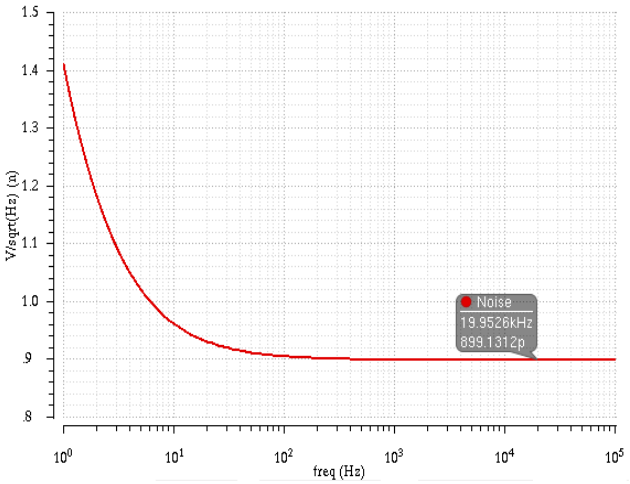


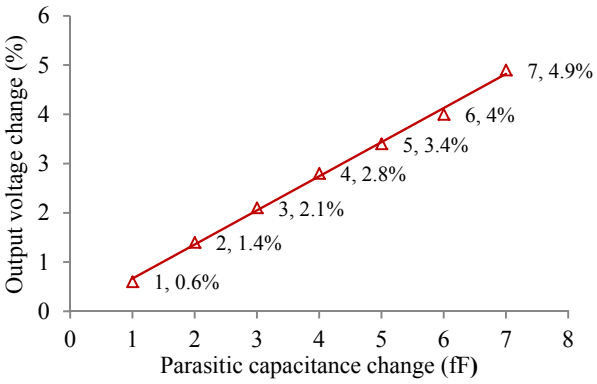
Figure 7. Total input inferred noise

To study the impact of parasitic capacitance variation on the proposed circuit performance, the sensing capacitance value was fixed at two different values (0.035 aF and 3.75 fF) and the parasitic capacitance was made to vary while the amplified output voltage was recorded and compared to the initial original output value to compute the percentile change, based on Equation 7.

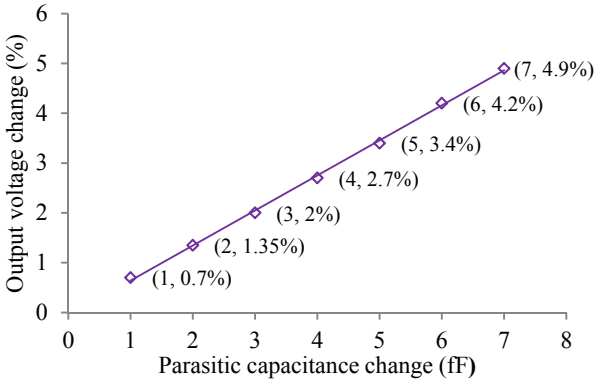
$$V_{o\%change} = \frac{|V_{onew} - V_{oold}|}{V_{oold}} \times 100\% \tag{7}$$

where, $V_{o\%change}$ is the percentage change in the output voltage, V_{onew} is the new output voltage after the parasitic capacitance variation and V_{oold} is the original output voltage prior to the parasitic capacitance change.

Simulation result showed that the percentage changes in the output voltage for both cases are almost identical and even when the parasitic capacitance changes by magnitudes much greater than the sensed signal, the percentage changes in the output voltage reading is about 5 percent only. Figure 8 shows the percentage output voltage change versus the parasitic capacitance change simulation results.



(a) 0.0375 aF



(b) 3.75 fF

Figure 8. Simulated parasitic capacitance change vs percentage change in output voltage

Besides, simulation result for a 10 aF sensing capacitance value showed that, the interface circuit is able to deliver an output voltage of 21.6 μV inferring the sensitivity of the interface circuit to be 2.16 μV/aF. Table 1 gives the performance comparison of the proposed interface circuit with reported past works of CMOS MEMS sensor applications. The result shows that the input referred noise performance of this work is much better compared to the other works referenced. However since its total gain, compared to the other works, is small it should be incorporated with additional amplifier stage to get a decent output signals. Hence it is ideal to be used

for CMOS MEMS sensor applications demanding low noise interface circuits with multi stage amplification. Further, Table 1 shows the power consumption is of this work is reasonable compared to the past works mentioned.

Table 1. Performance comparisons with reference works

Specification	This work	(Fang, 2006)	(Hu & Sawan, 2002)	(Saberhosseini, Zabihian, & Sodagar, 2012)
Supply voltage	3.3	3.3	1.8	3
DC Gain (dB)	18	20	51	62
Load capacitance (pF)	1	0.5	-	1
Noise stabilization technique	Chopper	Chopper	Chopper	-
Input-Referred noise (n V/√Hz)	0.9	12	56	59
Power consumption (mW)	0.3	0.396	0.775	0.004
Technology (μm)	0.35	0.35	0.35	0.5

4. Conclusion

A simple chopper stabilized cascode amplifier with both low-noise and low-power consumption qualities suitable for sub-atto farad CMOS MEMS capacitive sensing read-out circuit is presented. The proposed amplifier circuit can detect capacitance changes as low as 0.0375 aF and features good linearity up to 37.5 fF. It has an input inferred noise of 0.9 nV/√Hz and a power consumption of 0.33 mW. The amplifier circuit may be applied in monolithically integrated CMOS MEMS accelerometers, gyroscopes and chemical sensors as front end readout circuit where ultra-low capacitive changes need to be sensed.

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