On Board Computer Module for Cubesat Compatible with QB50

César A. Perdomo[1], Julián R. Camargo[1] & Albeiro Cortes Cabezas[2]

[1] Faculty of Engineering, Universidad Distrital Francisco José de Caldas, Bogota, Colombia

[2] Faculty of Engineering, Universidad Surcolombiana, Neiva, Colombia

Correspondence: César A. Perdomo, Faculty of Engineering, Universidad Distrital Francisco José de Caldas, Bogota, Colombia. Tel: 57-315-816-8303. E-mail: cperdomo@correo.udistrital.edu.co

Abstract

This paper presents the design and implementation at the hardware level of the OBC-OBDH subsystem (On-Board-Computer On-Board Data Handler) to meet the requirements of the CubeSat QB50 project, in addition, different tasks are performed at the software level to simplify the subsequent development (the implementation of the FreeRTOS real-time operating system has been carried out, and a simple example has been prepared that involves the use of all the necessary modules). The development of this module is justifiable at an academic level, since the QB50 project impacts on different aspects the academy (development of satellite systems), it must be taken into account that the QB50 challenge is presented to all the universities of the world and has a great impact on third world countries, providing the possibility of massive development and low launch costs.

Keywords: OBC, cubesat, QB50, FreeRTOS

1. Introduction

The QB50 project is a challenge that arises with the aim of studying the temporal and spatial variations of a series of components and key parameters in the lower thermosphere (90 to 320 km) with a network of about 50 double CubeSat, separated by a few hundreds of kilometers, which carry identical sensorics.

It also aims to study the reentry process by measuring a series of key parameters during reentry and by comparing the predicted, real CubeSat trajectories and orbital life times.

To participate in this project you can buy the different subsystems, some of which are endorsed by the promoters of QB50, which although they fulfill many of the project's requirements, leave their own missions unresolved and complicate the development with proprietary systems unknown until the moment of made the purchase.

The development of the first prototype of the OBC-OBDH (On-Board-Computer On-Board Data Handler) module that allows preliminary control tests on the different modules that interact within the CubeSat is considered.

The high costs of the OBC modules offered by commercial companies, and the requirement of high knowledge in real-time operating systems of the manufacturer, are a barrier to the development of systems that intend to use their own applications or from other manufacturers, taking into account that it is intended to use customized cards for the QB50 project that meet different needs, there is an obligation to stick to protocols and standards offered by these manufacturers. It is of vital importance to highlight the fact of developing own aerospace technology, using free tools as much as possible.

The CubeSat project, which began in 1999, began with the collaboration of professors from the California Polytechnic State University (Cal Poly), The Space Systems Design Laboratory at Stanford University (SSDL, Stanford University).

Multiple works related to the subject have been developed such as the one entitled *Designing on board Computer and Payload Dor the AAU Cubesat* in which he describes the design of the OBC module (On Board Computer) and the camera as a payload for the CubeSat AAU (Hedegard et al. al, 2008), or the one presented by Razzaghi in his thesis whose objective was to design and qualify an OBC module to meet the requirements of the system and the mission of Aalto-1 (Razzahi, 2012). The design and development of the OBC module suitable for ADCS applications is described in the thesis entitled *The Design and Development of an ADCS OBC for a CubeSat* (Botma, 2012).

The purpose of this project is to provide a standard for the design of peak satellites, to reduce the cost and time of development, increasing the accessibility to the space and the sustenance of frequent launches. Currently the Cubesat project, is an international collaboration of more than 100 universities, colleges and private firms developing peak satellites that contain science missions, private and for government use. A Cubesat is a cube of 10 cm, with a mass of plus or minus 1.33 kg, In general the standard determines a series of parameters at the physical level, size and mass of the satellite peak, in addition to a series of mechanical tests (vibration, temperature, crash test, visual inspection and test philosophy), which must be overcome for pre-launch acceptance. The launch is made with a standardized system, the pico-satellites (P-POD) Poly launch system (CubeSat California Polytechnic State University, 2015).

2. Method

2.1 Module OBC and OBDH

A CubeSat type system, typically consists of certain subsystems, each with certain specific functionality. There is a module that is responsible for feeding the entire satellite peak, called power, another is responsible for determining and controlling the attitude of the satellite (ADCS), the subsystem whose main mission is to establish the communication link with the segment of Earth is the call of communications, there is usually an OBC system, which is responsible for managing information between systems and in many cases also handles the payload of the system (PayLoad).

For any satellite, the OBC / OBDH module is considered the brain of the satellite, is responsible for managing and directing the various resources of the system. It also has the task of intercommunicating the different modules. Although each module has some independence, it is also obliged to report certain variables to the central OBC module, as well as having the capacity to make requests either from resources or from information from other modules (Rani et al, 2010).

The OBC module is in charge of keeping all the systems within the satellite in sync, in addition to synchronizing with the base station or in some way obtaining clock information with a certain level of precision and accuracy.

The state of the satellite (terrestrial transmission, Emergency, StandBy, among others), is the responsibility of the satellite, as well as determining the energy levels of the system's power module for each state. The Basic functionality of the OBC module is shown in Figure 1. The protocol that is used inside the satellite, is usually I2C, other bus types can arise based on CAN, SPI, RS232.
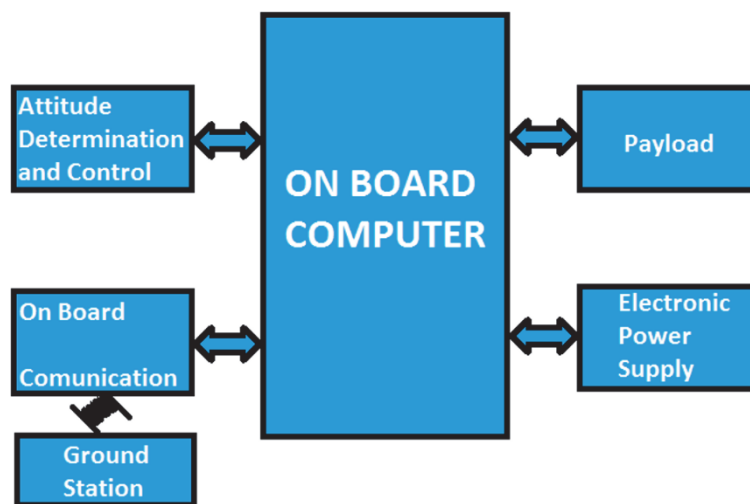

Figure 1. Functional architecture of the OBC module (Rani et al., 2010)

In addition to performing inter-modular tasks, in some cases it is required that the OBC module perform other tasks. They can be arithmetic calculations to free up load on other modules, as well as perform storage tasks. Some projects, such as QB50, request more than one memory system (2 SD memories) in this module.

2.2 Especificaciones del sistema OBC-OBDH

It is based on the fact that the OBC-OBDH module for the CubeSat QB50 system must manage the information requested and deliver all subsystems within the CubeSat (Power, Attitude, Communications and Payload), in

addition to storing the orbital packets and respective to the science unit while it is not discharged in the ground segment.

Based on previous studies (Masutti et al., 2014), the scheme shown in Figure 2 is generated, and since the same satellite within the ADCS module (attitude determination and control module) has a GPS of high precision, it will not be necessary to locate another one in the designed module.
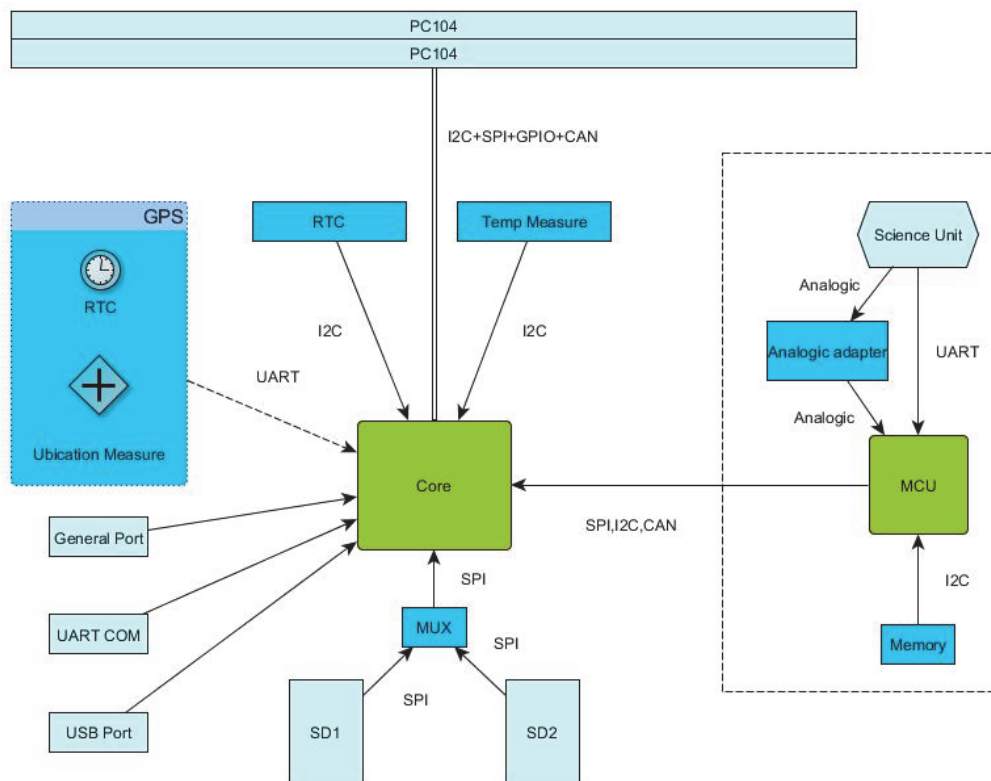

Figure 2. General scheme OBC-OBDH for QB50

Then, taking into account the general scheme, we proceed to describe the series of module specifications:

- Real Time Clock (RTC)
- Temperature sensor
- 2 SD Card interfaces (or microSD Card)
- USB connection
- Serial debugging connection (or umbilical cable)
- Programming connection
- Compatible device CubeSat Kit
- Bus Compatible CubeSat Bus Kit
- Bus compatible with QG50-UD connections
- PCB compatible with CubeSat specification PCB Kit
- Layout and operation compatible with CubeSat standard
- Layout for RBL and LS switches (Remove Before Launch and Launch Switch)
- Port / Connector available for interface with science unit
- Processing capacity for the management of 2 SD memories, as well as the capacity to manage information in real time of the other subsystems
- Consumption less than 500mA (Average current on the bus of 5V-3.3V)

2.3 Schemes and Systems Utilization

2.3.1 Memories type SD/MMC

It is necessary to store in two SD memories the information that has not been downloaded to the earth station segment. The connection with the microcontroller used will be made through the SPI module thereof, as shown in Figure 3.
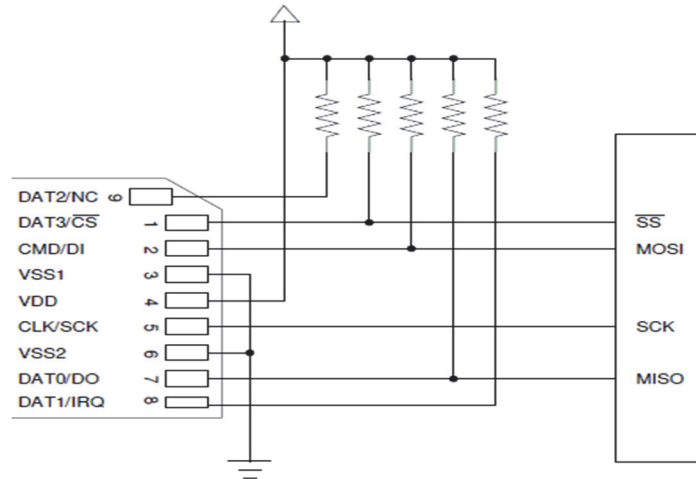

Figure 3. Connection SPI-SD Card

Since it is not necessary to write or read in the two memories at the same time, a switching model is described below. Although the memories are based on SPI communication (where there is a CS selection line), the consumption of the data must be taken into account. if they remain on, so it is proposed to keep the MISO, MOSI, SCK and CS lines in common for the two memories, and turn the memories on and off at different times with a control circuit as shown in Figure 4.
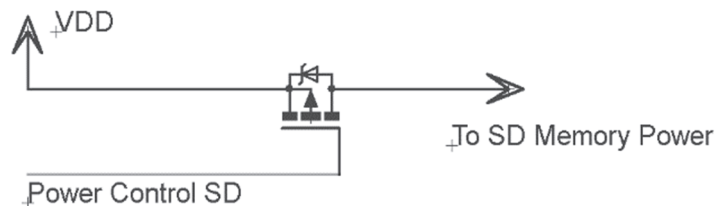

Figure 4. Power circuit SD memory

For such a process, a P-type MOS-FET transistor with very low switching resistance and related circuitry can be used, but there are packaged solutions that require fewer external elements, the reference component TPS222929 (Ultra-Small Low on Resistance Load). Switch with Controlled Turn-on), allows such functionality, and a typical application is shown in Figure 5.
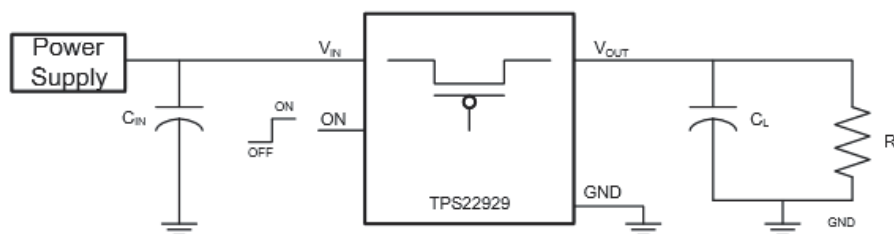

Figure 5. Typical application TPS22929 (Texas Instruments, 2014)

2.3.2 RTC Module

The real-time module (RTC) should only comply with the 500ms error requirement established by the project, to avoid complications due to the availability of ports, access from parallel manufacturers, serial port, SPI, I2C, and others are offered by different manufacturers. , an internal bus has been determined for the OBC type I2C module

to connect this peripheral and the temperature sensor (if necessary).

The BQ32000 real-time reference clock, supports I2C type connection with a clock at 400kHz, requires a crystal of 32,768 kHz and comes packaged in 8-pin SOIC which makes it perfect for the card. It is also capable of generating a signal of interruption by time at 1Hz and 512Hz (Texas Instruments, 2015), which allows it to be used to wake up the microcontroller or some other peripheral.

2.3.3 Thermal sensor

It is necessary to know the temperature of the module in general, and for this the temperature sensor of the microcontroller can be used, but it has been decided that to have a better response an external temperature sensor is necessary.

It was decided to use an I2C type interface for all the elements of the module (RTC, temperature sensor), so the LM75A sensor was chosen, which does not require external elements and handles this type of interface. The temperature range of the sensor is from -55ºC to 125ºC, making use of a 9-bit word.

2.4 Module Interfaces

It is necessary to have some connections inside the module to be the interface with the additional elements (Science Unit, Debug Unit, Programming unit, and others).

2.4.1 Connector for science unit

As the science data must be stored directly in the OBC module, a generic connector must be established. The development of this connector is pending, since the card by the research group has not yet been designed.

In the same way it is known that the interface contains communication pins Serial type UART and possibly a DAC with I2C interface.

2.4.2 Connector for Umbilical Cord

A USB port and serial communication are available directly from the OBC module to allow direct information. The USB communication operates in the same way as for the CubeSat Kit, and a serial interface close to the debug side.

2.4.3 Programming Connector

To program the Microcontroller, you must have a physical J-TAG connection, which is composed of the TCK, TMS, TDI, TDO and RST signals of the device, as well as power and ground lines. A 2x5 molex type connector is used for this purpose, taking into account as a reference the mikroProg for Tiva C solution and the specification given directly by Texas Instruments (Ashara, 2016). In Figure 6, the general scheme that is going to be taken into account as a reference for the design is shown.
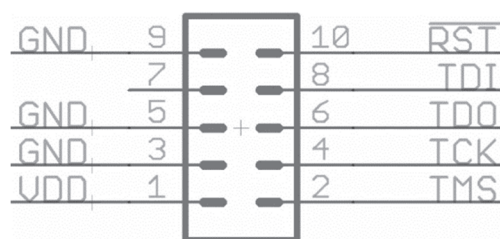

Figure 6. J-TAG connector for programming

2.5 Circuit Diagrams and Design Considerations of the Card Implemented

Figure 7 shows the circuit diagram of the design made for the OBC-OBDH QB50 card, in the image you can clearly differentiate each of the blocks shown above in Figure 2.

As a basis for the printed circuit design, the document *System Design Guidelines for the TM4C123x Family of Tiva C Series Microcontrollers* prepared by Ken Krakow, Sheldon Johnson and Jonathan Guy was taken into account as an application report (Krakow, 2013), as well as a series of books and articles that were taken into account to avoid electromagnetic radiation by the handling of high frequencies within the circuit.

For purposes of capacity and good practices, the document IPC-2221A, *Generic Standard on Printed Board Design* (IPC, 2003) is taken into account, which allows to guarantee certain measures for the correct operation of the printed circuit.
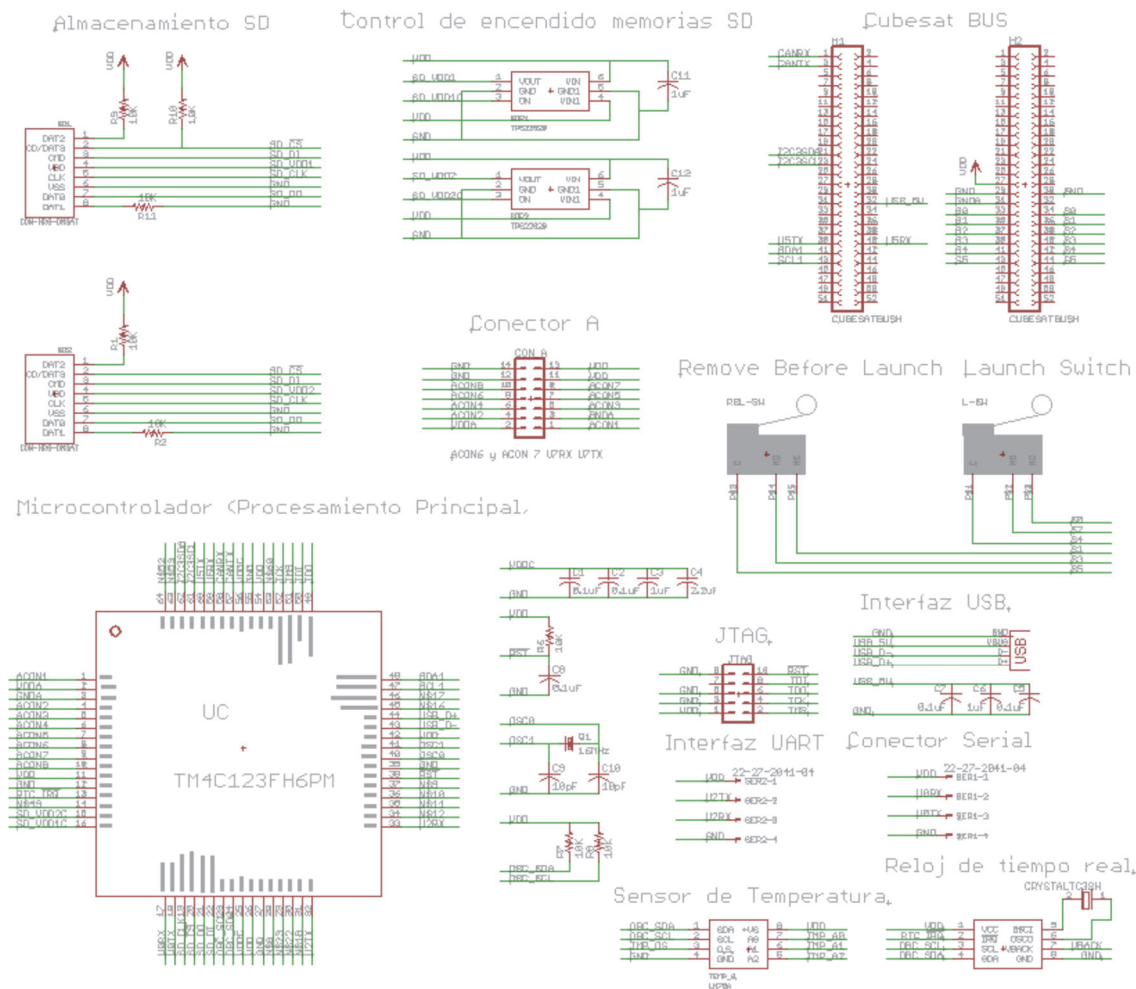
Figure 7. Circuit diagram of the OBC-QB50 card

It has been taken into account that the complete design will be located inside a metal box, which largely isolates the electromagnetic and thermal radiation. The complete design is done with the EAGLE software tool, making use of the CadSoft Freeware license, other tools were considered as KiCad or Altium Designer, but the design in Eagle is known to the authors, and the design requirements can be be handled in CadSoft's EAGLE.

In the standard, it is determined that the CubeSat must have the center of mass in a sphere of diameter 2mm with respect to the physical center, being that the location of the heavier components (besides the CubeSat Bus kit) as USB port Remove Before Launch Switch and sockets for the microSD Card memories must be located in such a way that the center of mass is not affected. As already determined, within the OBC module (Figure 8), the corresponding connectors must go to:

- USB -B Connector (Direct USB Interface -OBC for testing)
- JTAG Connector (Programming Interface and Microcontroller debugging)
- SER 1 Connector (Serial Interface for debugging the system)
- SER 2 Connector (Serial Interface to connect Peripherals or Payload)
- RBL -SW Connector (Remove Before Launch Switch)
- L -SW Connector (Launch Switch)
- CON-Peripheral Connector (Science Unity).
- SD -1 WITH Connector for SD Memory 1
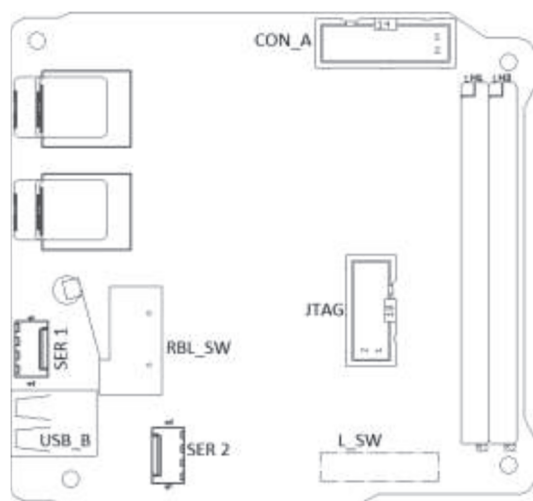- SD -2 WITH Connector for SD Memory 2

Figure 8. Arrangement of connectors on the OBC-QB50 card

Three independent track widths were used, the first one has all the digital logic and the microcontroller connections, the second is only for the charge power of the batteries (5V of the USB port), and the third is for the interface between the RBL and LS switches with the Bus CubeSat Kit.

Making use of the method used by the company Eycom in the tables of the IPC-2224A (Piñeiro, 2011), the need for a great thickness in the tracks is seen, since to be able to access the PC-104, a certain width must be respected If this is omitted, short circuits may appear on the bus, which is a serious problem for the design. Below are the graphs to start the design (Figure 9 y Figure 10).
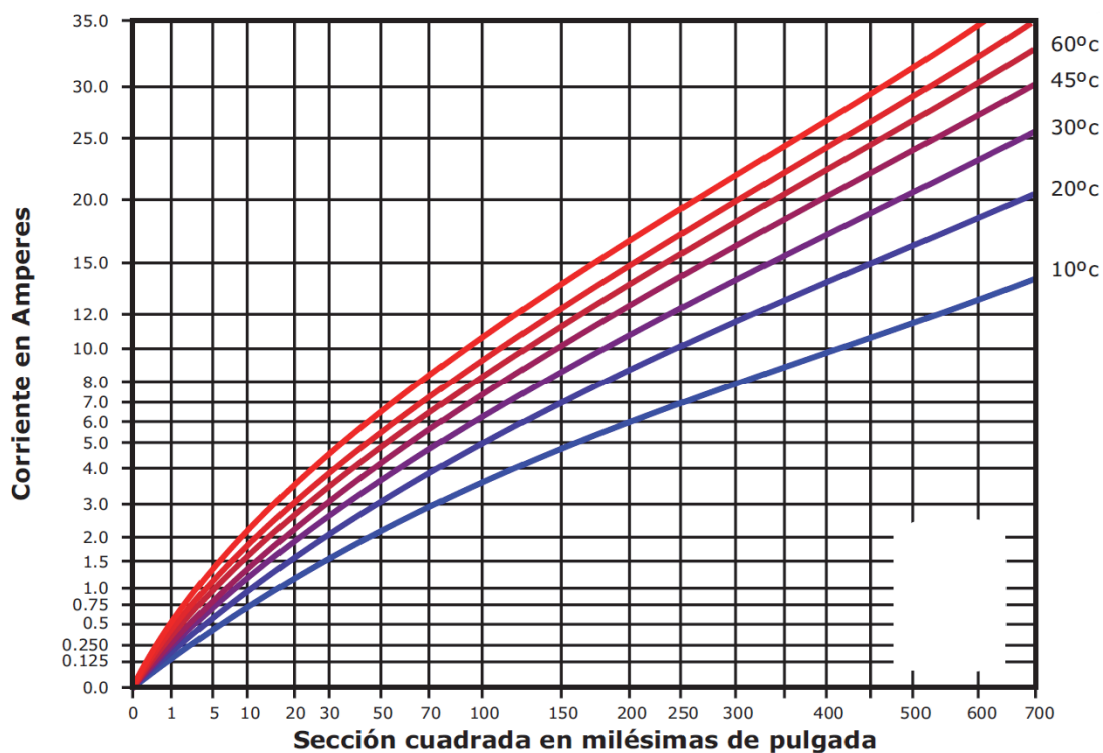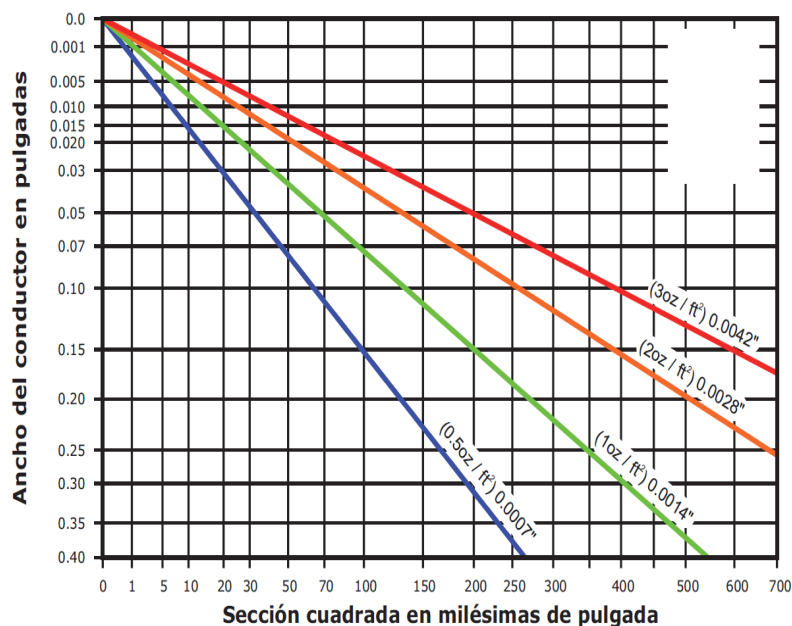

Figure 9. External conditions

Figure 10. Width of the conductor in relation to the cross section

Microcontroller connections: The thickness requirement for these connections is maximum 100mA, it is observed in Figure 9 that for an increase of 10ºC, we have a square section of approximately 5 thousandths of an inch, and in Figure 10, that the width of the driver is of the order of 0.001-0.01 inches.

Power load connections: The thickness requirement for these connections is of maximum 900mA, it is observed in Figure 9 that for an increase of 10º C, there is a square section of approximately 17 thousandths of an inch. In Figure 10 it can be seen that the width of the conductor is of the order of 15 thousandths of an inch for a plate with 1oz / ft2, which shows the need to use said copper concentration in the plate.

Connections for switches RBL and LS: The thickness requirement for these connections is of maximum 2A, it is observed in Figure 9 that for an increase of 10ºC, we have a square section of approximately 50 thousandths of an inch. And in Figure 10the conductor width is of the order of 30 thousandths of an inch for a plate with 1oz / ft2.

In Figure 11 and Figure 12 you can see a real image of the OBC-QB50 card both for the face of components and for the welding face respectively.
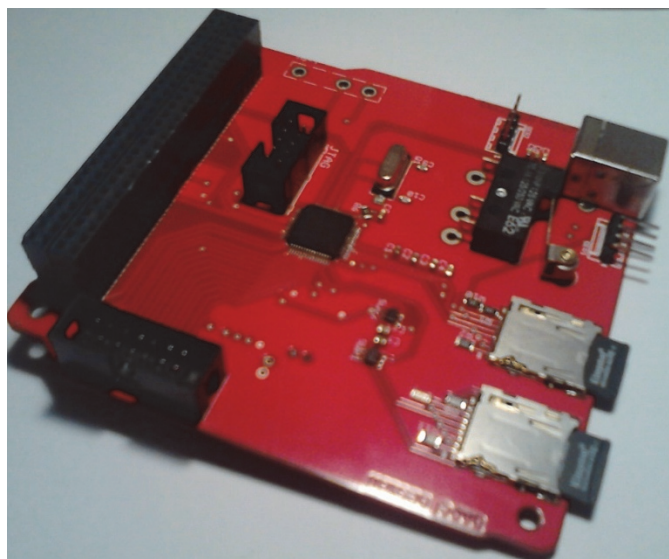

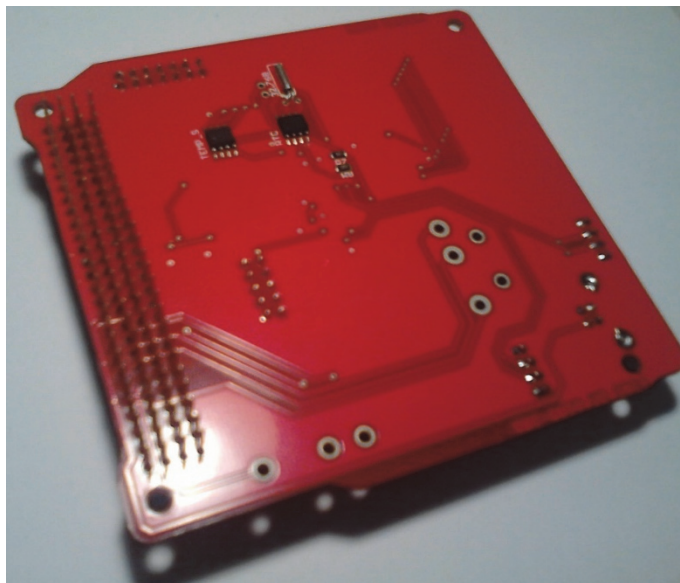Figure 11. Photograph of the OBC-QB50 card face components

Figure 12. Photograph of the card OBC-QB50 welding face

3. Results

3.1 Test Programming and Debugging in the Circuit (JTAG)

By using a programming and / or debugging tool, it is verified that the central core of the OBC module is being written correctly in the Microcontroller. As a physical programming medium, the JTAG connector available on the Texas Instruments development platform (Stellaris Launchpad) is used. In Fig. 10, the actual assembly where the tests were performed is shown, where (1) corresponds to the JTAG connection, (2) microcontroller power and ground, (3) target microcontroller, (4) development platform and JTAG programmer.

With the Texas Instruments programming tool (LM Flash Programmer- Build 1588), the microcontroller was programmed, then the memory is read and stored in the desktop memory. It can be concluded that although some tests had problems the type of packaging of the microcontroller makes it difficult to perform tests, access to a card like the one shown in Figure 13 (right part of the image) facilitates the assembly by converting the surface packaging to a 5mm pin layout.
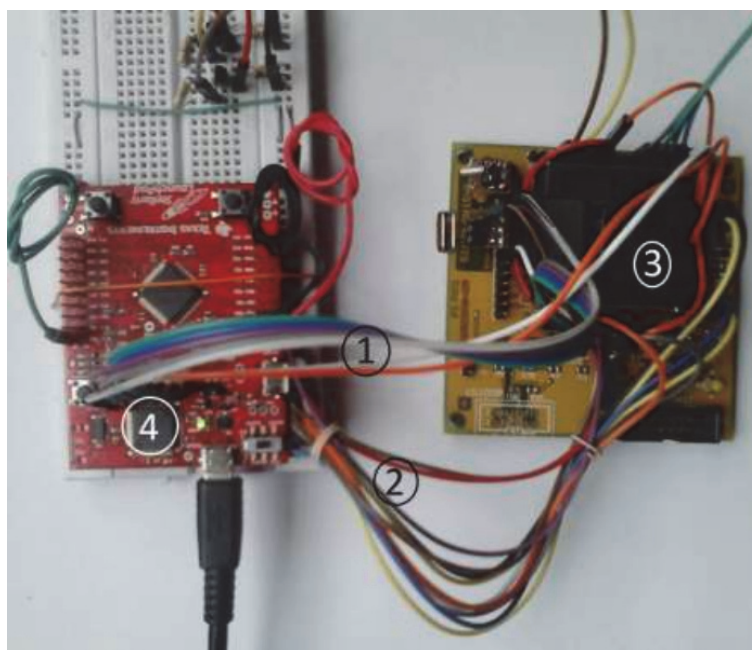

Figure 13. Physical assembly of test

3.2 Consumption Test and Correct Operation

Test Determination: Current tests were carried out to determine the maximum consumption of the device, which were the most influential factors in said consumption and finally the correct or incorrect operation of the design was determined.

Test execution: To carry out the test, the assembly of Figure 14 was implemented and the microcontroller was programmed following the steps of the previous test. This shows the complete assembly, where (1) corresponds to the I2C circuit, (2) connection circuit of the SD memories and (3) Serial Communication.
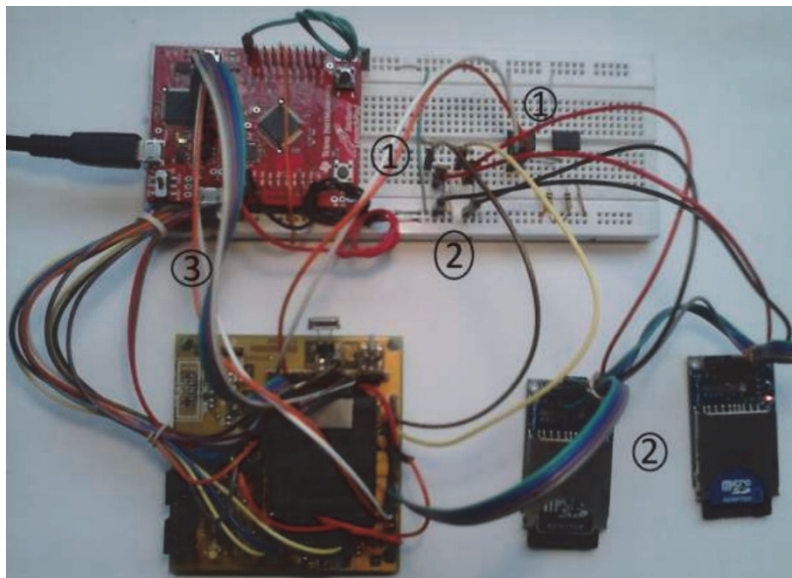

Figure 14. Mounting Test 2

It must be borne in mind that the measurements for the consumption of SD memories have a slight increase, due to the card used (it has an LED indicator, consumes a current of 5.25 mA for a voltage of 3.32 V). The first test carried out makes use of the complete SD Memory Reading and writing code, and was carried out in order to analyze the consumption of the memory in different states: without power (Control circuit), on, in reading and during file writing . The following results were obtained: Off: 4.21mA, StandBy: 9.95mA, Reading: 11.79mA and Writing: 42.3mA.

The consumption of the microcontroller was evaluated without connection of peripherals (memories SD temperature sensor or RTC) was executed the same source code of the previous case. Taking into account that no level of low consumption or sleep is entered in the microcontroller, it was established that the average current is 19.95 mA, since it varies in short periods of time (while receiving and transmitting through the serial port) .

Finally, the test was conducted to the I2C bus, where the main code was modified, and one was included to configure the module, initiate a communication, send 4 data and finalize the communication. The consumption of the power circuit for the I2C devices was 11.5mA (taking into account the pull-up resistors). And during the writing there were no significant changes in diet (+/- 785 uA).

The entire circuit was measured, and 105.3 mA was obtained as the maximum peak when writing to the microSD memory.

4. Conclusions

It is possible to design the hardware level of the OBC-OBDH subsystem compatible with the requirements of the CubeSat QB50 project, which meets the functionality, efficiency and performance requirements necessary to be included in the QB50-UD development. Although the implementation of 4-layer printed circuits represents high costs, the idea is sustainable, taking into account the benefits obtained in terms of stability and requirements for high-speed communications.

Although there have been more developments of this type of modules (OBC), the fact of carrying out the complete design from the hardware level, allows a wide flexibility to support missions (a design for multiple launches).

The energy levels required by the system allow a wide expansion of the module (including more processing cores, external memories, FPGA, among others), which opens the way to a greater capacity for the management of missions.

The developed system can be taken into account for terrestrial systems, since it opens the field for the use of multiple communication protocols, in addition to having large processing capacities.

Making changes that do not involve much development time, you can use the study in this project to design other functional modules compatible with CubeSat.

Acknowledgments

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