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Predictive Reliability Model of 10G/25G Mesa-Type Avalanche Photodiode Degradation

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Abstract

Avalanche photodiodes (APDs) are important building blocks for high-sensivity, low-noise receivers deployed in the datacenter, wireless and cloud computing networks. Maintaining stable dark current is a crucial task for overall robust sysem reliability. To achieve design-in low dark current stability, good knowledge of reliability physics is indispensable. In this work, we study the physical mechanisms of 10G/25G mesa-type APD degradation. We institute a predictive reliability model to account for the degradation processes. A comprehensive comparison of APD and IC transistor is also illustrated in terms of dielectric breakdown, mobile ion migration and hot carrier injection. The model suggests that surface leakage current is the dominant factor for the mesa-type APD degradation. Based on the model, it is predicted that highly reliable 10G/25G APD can be achieved with the suppression of weak links at the surface/interface states.

Keywords: semiconductor, reliability model, avalanche photodiode, reliability physics, dielectric breakdown, mobile ion, hot carrier injection

1. Introduction

Semiconductor photodiodes are important building blocks for the high-sensitivity receivers deployed in the 2.5 and 10G optical communication systems such as passive optical network (PON) and local area networks (LAN) (Ishimura et al., 2007). The recent development of datacenter networking, wireless and cloud computing have further fueled the demand for the high-performance receivers.

Among the photodiode portfolio, APDs are attractive devices due to the signficiant improvement in photoreceiver sensivity compared with traditional p-i-n (PIN) photodiodes (Achouche et al., 2010). By adding the multiplication layer, the avalanche photodiodes combine the detection and amplification properties simultaneously. However, the high electric field in the avalanche region often imposes a reliability concern.

Recently, 10G/25G APD has drawn increasing interest in the market place due to the high-bandwidth and low-noise performance advantages. In order to achieve the high bandwidth, a mesa structure with both P and N electrodes on the top surface is typically employed (Kim et al., 2001; Takeshita et al., 2006; Watanabe et al., 1996; Smith et al., 2009). One of the key challenges though is to maintain low dark current over time. Compared to semiconductor lasers (Huang et al., 2016; Twu et al., 1993; DeChiaro et al., 1992), there was relatively scarce amount of reliability work conducted on the APD (Ishimura et al., 2007; Kim et al., 2001; Watanabe et al., 1996). In this paper, we study the physical degradation mechanisms of 10G/25G mesa-type APD. We present the predictive reliability model for the degradation processes and suggest that the surface leakage current is dominant for the mesa-type APD. The model predicts that highly reliable 10G/25G APD devices can be achieved with the suppression of the weak links.

2. Experimental

The reliability model was based on the schematic of the 10G/25G mesa-type APD structure shown in Figure 1. The APD structures considered in the model included the N-mesa at the bottom, the active region in the middle and the P-mesa at the top. The N-mesa consisted of the N-InP buffer and contact layers. The active region consisted of the InAlAs multiplication, the graded quaternary (Q) layer and the absorption layer. The P-mesa consisted of the p-InAlAs window and p-InGaAs contact layers. To achieve the 10G high-speed, the mesa-type

APD was formed where both P and N electrodes were on the top surface. The p-contact was made by forming the metal ring immediately outside the anti-reflective (AR) window. The p-ring was connected to the outside p-pad by the metal bridge. The n-metal contact was connected to the N-mesa. For the passivation, the model considered the low-k dielectric material such as polyimide.

Since the mesa-type APD typically exhibited higher degradation rate than the planar type (Kim et al., 2001; Watanabe et al, 1996), the model focused on the surface leakage at the semiconductor/dielectric interface. The reliability model discussed the effects of dielectric breakdown, mobile ion migration and hot carrier injection.

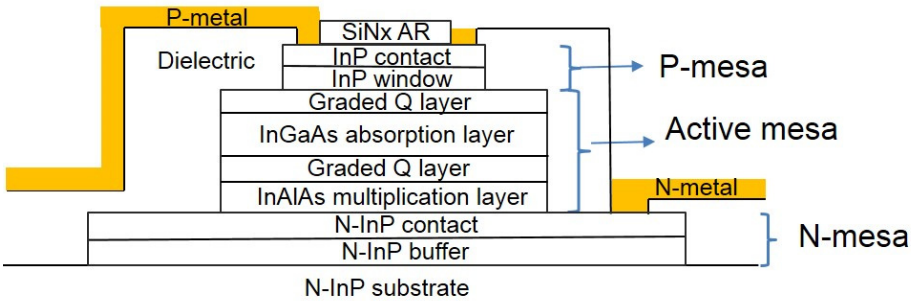

Figure 1. Schematic of 10G/25G mesa-type APD structure used in the reliability model

3. Results and Discussions

The typical APD degradation for long-term wear-out is characterized with the increase in dark current over time. The dark current variation, $[I_d(t)-I_d(0)]/I_d(0)$, can be expressed in the following empirical terms shown in Equation (1). The first term accounts for the stress current dependence where the K_I is the normalization constant, I_r is the reverse current applied to the APD during aging and N is the current exponent for the acceleration factor. The second term relates to the stress temperature dependence where E_a is the activation energy, k is the Boltzmann's constant and T is the temperature. The third term describes the aging curve where a is the fitting constant that determines the failure time, t is the aging time and m is the fitting parameter. The temperature and current dependences in Equation (1) are similar to the Black's equation where the mean-time-to-failure (MTTF) follows the reciprocal of the first two terms (Black, 1969; Huang, 2005).

$$\frac{I_d(t)-I_d(0)}{I_d(0)} = K_I I_r^{\ N} \exp(-\frac{E_a}{kT}) a t^m \tag{1}$$

For the current exponent, two stress currents can theoretically determine the N value. In practice, estimates based on three currents are more reliable since the confidence level is higher. However, one has to ensure that no new failure mechanism is introduced at the increased current density to avoid electrical overstress (Huang et al., 2007; Huang, 2015). The other alternative method of bias aging involves reverse voltage bias. The empirical equation can be modified as shown in Equation (2) where K_V is the normalization constant and V_r is the reverse voltage bias.

$$\frac{I_d(t)-I_d(0)}{I_d(0)} = K_V V_r^{\ N} \exp(-\frac{E_a}{kT}) a t^m \tag{2}$$

For the activation energy, two stress temperatures in principle can determine the E_a value. In practice, estimates based on three temperatures are more reliable due to the higher confidence level. Again, the elevated temperature for the aging test needs to be carefully designed in order to avoid unwanted new failure mechanism. The typical stress temperature is in the range of 60 to 200°C for APD aging.

For the fitting of degradation curves, the polynomial function has been employed to describe the aging behaviors of both lasers (Sim, 1989; Huang et al., 2005) and photodiodes (Kuhara et al., 1986). Typically, the sublinear model provides more accurate fit. In the sublinear model, the experimental curve is fitted by the equation where the exponent *m* is varied until the best correlation is found. The constant *a* is then deduced to determine the failure time.

Owing to the larger amount of reliability studies for the laser diodes, there have been several models established to describe the degradation behavior over aging time. For example, the Sim model (Sim, 1989) was based on a polynomial function. The polynomial expression provided good description for the late stage of degradation, and it has also been widely accepted by Telcordia and telecommunication communities. The Chuang (Chuang et al., 1998) and Lam (Lam et al., 2003) models were based on exponential functions and offered good description for the early stage of degradation. The exponential term was derived from the rate equation assuming that the degradation rate was proportional to the defect density.

$$I_d = I_{dd} + I_{dt} + I_{dg} + I_{ds} \quad (3)$$

For the APD degradation, the most common feature is associated with the increase in dark current. The total dark current can be expressed in Equation (3) where I_{dd} is the diffusion current, I_{dt} is the tunneling current, I_{dg} is the generation current and I_{ds} is the surface leakage current (Ohnaka et al., 1987; Fukuda, 1999). The diffusion current ideally corresponds to the saturation current and is typically determined by the epitaxial layers and design. The tunneling and generation currents are also largely pre-determined by the epitaxial layers. For the mesa-type APD structures, the surface leakage current (I_{ds}) is the dominant factor due to the presence of the interface states or traps between the dielectric film and the semiconductor. As shown in Equation (4), the surface leakage current becomes more pronounced after aging due to the weak-link nature near the surface/interface of the passivation/semiconductor. The surface and interface states could easily trap defects or carriers to cause the leakage current to increase. Any surface leakage current flows via the p-n junction at the defective surface or interface site would contribute to the dark current.

$$I_d(t) \sim I_{ds}(t) \quad (4)$$

In the following, we discuss the degradation mechanisms that could be responsible for the surface leakage current. Due to the larger number of research papers in the ICs (Fang et al., 2014; Lee et al., 1995; Kufluoglu et al., 2006; Heremans et al., 1988; Hu, 2009), we will also compare the APD degradation components with those of the IC transistor in order to shed some light on the APD reliability. We highlight the similarities in terms of dielectric breakdown, mobile ion migration and hot carrier injection in Sections (a)-(c).

(a) Dielectric breakdown (DB)

For the high-speed APD, low-k dielectric material is often employed in the passivation. However, the low-k passivation imposes a reliability concern due to two main reasons. First, the low-k dielectrics such as polyimide and benzocyclobutene (BCB) exhibit lower dielectric strength than that for the SiO_2 or SiN_x (Franssila, 2010; El-Kareh, 1995). For example, the dielectric strengths for the low-k polyimide and BCB are around 1.2-2.5 and 3.0MV/cm, respectively. On the other hand, the dielectric strengths for SiO_2 and SiN_x are around 10-12MV/cm. Secondly, the dielectric strength for the passivation thin film on the APD device is expected to be lower than that rated for the bulk. For the passivation film, the breakdown failure may be enhanced by the high electric field near the depletion region as well as the localized inhomogeneity on the mesa surface, as shown in Figure 2a. During the APD aging, the traps are initially formed in scattered manner in the dielectric film. As more and more traps are created, they start to connect and form conduction path. Once the conduction path is developed, localized heat would be generated, leading to thermal damage (Ma, 2009). The heat would further accelerate additional formation of traps and development of conduction path in a positive feedback loop, eventually leading to thermal runaway.

The surface leakage current associated with the dielectric breakdown could be expressed by the thermochemical "E" model or the anode hole injection "1/E" model (McPherson, 2012). For the "E" model, the dark current associated with the dielectric breakdown can be described in Equation (5) where A is a constant, γ is the field acceleration parameter, E is the dielectric field and ΔH is the enthalpy or activation energy required to break or coordinate the bonding of dielectric molecules. The model assumes that the defect generation in the dielectric film results from phonon-driven bond breakage/coordination process.

$$I_{ds}(DB_E) = A\exp(\gamma E - \frac{\Delta H}{kT}) \quad (5)$$

For the "1/E" model, the dielectric damage was assumed to result from the electrical conduction through the dielectric due to Fowler-Nordheim (F-N) mechanism (Fowler et al., 1928). The ionization process involving electron and hole injections was responsible for the dielectric damage or breakdown. The surface leakage current based on the "1/E" model followed the exponential dependence in Equation (6) where B is a constant, G is the tunneling factor and E is the dielectric field.

$$I_{ds}(DB_{1/E}) = BE^2 \exp(-\frac{G}{E}) \tag{6}$$

The high electric field near the depletion region of the avalanche layer or the localized mesa surface inhomogeneity may further aggravate the dielectric damage. The field-assisted conduction mechanism is called Poole-Frenkel effect (Frenkel, 1938). The P-F conduction in the dielectric can be generally expressed as Equation (7) where C is a constant, ϕ_B is the electron energy barrier, ε is the dynamic permittivity. The exponential term describes that the electron does not need as much thermal energy ($q\phi_B$) to get into the conduction band under the influence of electric field. In the high electric field, the energy barrier is significantly reduced to $q(\phi_B - \sqrt{qE/(\pi\varepsilon)})$.

$$I_{ds}(DB_{P-F}) = CE \exp(-\frac{q(\phi_B - \sqrt{qE/(\pi\varepsilon)})}{kT}) \tag{7}$$

For the complementary metal oxide semiconductor (CMOS) transistor, the gate dielectric leakage also occurs as a result of gate voltage stress. Time-dependent dielectric breakdown (TDDB) is commonly used terminology to describe the increase in the gate dielectric leakage due to the irreversible formation of electrically active defects. Those active defects form conductive percolation in the dielectric film that shorts the cathode and the anode, as shown in Figure 2b. The early phase of the dielectric breakdown is typically associated with the leakage current increase, characterized as "soft" breakdown. The later stage of the dielectric breakdown involves short failure, characterized as "hard" breakdown (Oates, 2015).

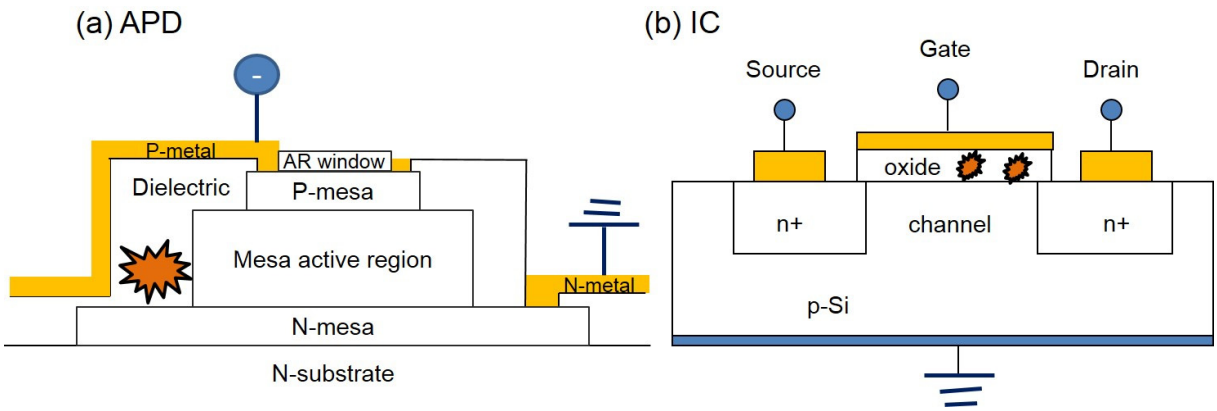

Figure 2. Schematics of degradation mechanisms of (a) APD dielectric breakdown and (b) IC gate oxide breakdown

As shown in Table I, the mechanism of the APD dielectric breakdown share some commonality with the ILD or gate dielectric breakdown in the integrated circuit (IC) transistor devices. For the ILD breakdown in the IC, the breakdown occurs along the interface between the low-k dielectric and its capping layer (Oates, 2015).

Table I. Dielectric breakdown of APD and its comparison with IC failure mechanism.

	APD	IC
Degradation pattern	Increase in dark current or short-circuit failure	Increase in the gate dielectric leakage or the interlevel dielectric (ILD) leakage
Physical mechanism	Low-k dielectric passivation breakdown	Low-k ILD breakdown Gate dielectric breakdown
Aging method	Reverse bias, typically involving negative stress current of 100μA at elevated temperature in the range of 60-200°C.	TDDB typically involving constant stress voltage applied to capacitor or transistor test structure at elevated temperature such as 150°C.

(b) Bias temperature instability (BTI)

The second potential root cause for the increase in dark current was related to the surface leakage current associated with mobile ion migration. For the polyimide passivation, there was some trace amount of impurities such as Na and Cu contained in the film (Watanabe et al., 1996; Pereira et al., 1993). Those impurities were likely to diffuse along the interface or into the passivation film driven by the high electric field at the depletion layer, as illustrated in Figure 3a. The mobile ion migration along the interface of the passivation and the semiconductor would result in the surface leakage current, leading to the increase in dark current. Brown (Brown, 1982) has reported that only 0.8ppm of sodium ions was enough to make polyimide a leaky dielectric. The density of the surface and interface states strongly depended upon device process and passivation method. The surface and interface states could easily trap carriers as generation-recombination centers.

The surface leakage current associated with the mobile ion migration can be expressed in Equation (8) where q is the charge of the mobile ion, A_s is the surface (interface) area of the p-n junction depletion region, n_m is the mobile ion density, σ_m is the capture cross section of mobile ions, υ_m is the thermal velocity of the mobile ion and N_{sm} is the trap density of mobile ions at the surface (interface).

$$I_{ds}(BTI) = (\frac{qA_s}{2})n_m\sigma_m\upsilon_m N_{sm} \tag{8}$$

In the metal oxide semiconductor field effect transistor (MOSFET), negative bias temperature instability (NBTI) manifests as an increase in the threshold voltage and consequent decrease in the drain current. The NBTI is most pronounced in the p-channel MOS (PMOS) due to the operation of negative gate-to-source voltage. The mechanism of NBTI is not completely clear. One plausible explanation is the hydrogen model that involves the hydrogen release from the Si dangling bonds at the SiO_2/Si interface (see Figure 3b), following the capture of a hole from the Si channel (Chakravarthi et al., 2004; Drapatz et al., 2009). The accumulation of the mobile species (H^0 and H^+ shown in Equations 9 and 10) can form the interface states or traps that are responsible for the NBTI degradation.

$$SiH + h^+ \Leftrightarrow Si^+ + H^0 \tag{9}$$

$$SiH + 2h^+ \Leftrightarrow Si^+ + H^+ \tag{10}$$

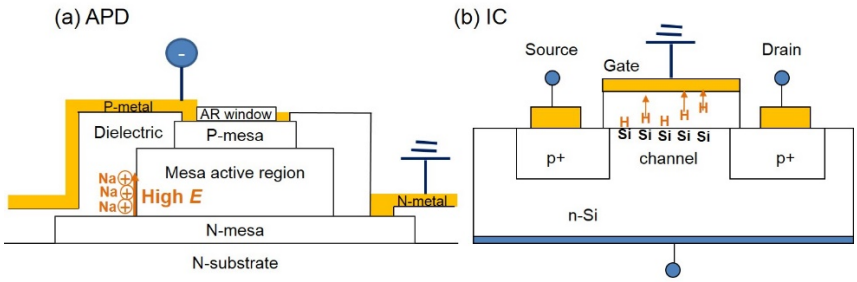

Figure 3. Schematics of degradation mechanisms of (a) APD mobile ion migration and (b) IC bias temperature instability

Table II. Mobile ion migration of APD and its comparison with IC failure mechanism.

	APD	IC
Degradation pattern	Dark current increase or short-circuit failure	Threshold voltage shift of PMOS due to NBTI or NMOS due to PBTI
Physical mechanism	Mobile ion accumulation (Na, Cu, etc.) from the polyimide and migration by the high electric field in the depletion layer	Positive charge generation due to hydrogen release from passivated Si dangling bond at the SiO_2/Si interface in the transistor
Aging method	Reverse bias, typically negative stress current of 100μA at 60-200°C.	DC stress involving the gate voltage and drain voltage at elevated temperature such as 150°C.

As shown in Table II, the mechanism of mobile ion migration such as Na in the polyimide passivation of the APD is similar to the mobile species migration such as H^0 and H^+ in the gate dielectric of the PMOS. The other similarity is the polarity of bias applied to the devices. For the APD, the p-contact is subjected to the negative bias. For the PMOS, the gate voltage is set in negative polarity relative to the source and drain voltages.

(c) Hot carrier injection (HCI)

The third mechanism for the increase in dark current of APD was related to hot carrier injection, as shown in Figure 4a. Under the relatively high electric field in the depletion layer, part of the thermally excited holes (hot holes) acquired sufficient energy to overcome the energy barrier and enter into the dielectric film (Sudo et al., 1988). When the holes entered the dielectric, they formed interface states and create positive surface charges. Upon the accumulation of the positive charge, the depletion region shrank gradually that made the field become more intense. The enhanced electric field would accelerate more hole injection, leading to positive thermal runaway.

The surface leakage current associated with the hot carrier injection can be expressed as Equation (11) where q is the carrier charge, n_i is the intrinsic carrier density, σ_i is the carrier capture cross section, υ_i is the carrier thermal velocity and N_{si} is the carrier trap density at the surface (interface).

$$I_{ds}(HCI) = (\frac{qA_s}{2})n_i\sigma_i\upsilon_i N_{si} \tag{11}$$

For the IC transistor, hot carrier degradation occurred as a result of high lateral field in the source/drain channel (see Figure 4b). As a result of vertical field in the gate, the holes and electrons were separated and either injected into the gate dielectric or ejected into the transistor substrate (Duncan et al., 1998).

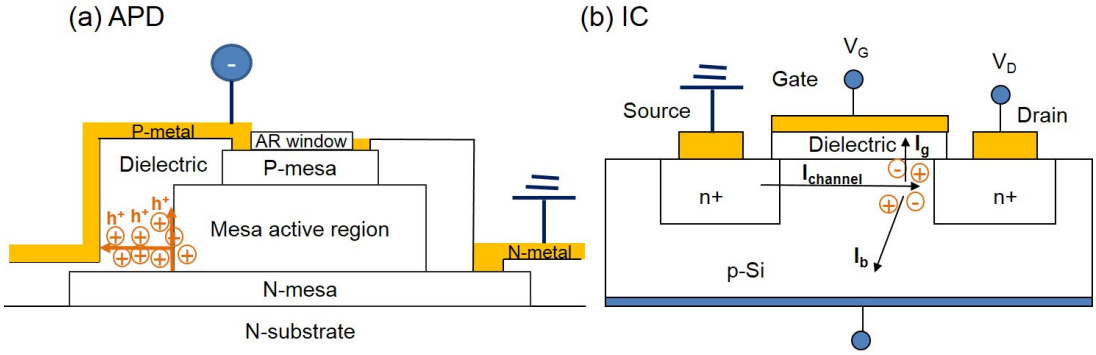

Figure 4. Schematics of degradation mechanisms of (a) APD hot hole injection and (b) IC hot carrier injection

As shown in Table III, the hot hole injection into the passivation dielectric of the APD is similar to the hot carrier injection into the gate oxide of the IC transistor. The carrier injection would result in the formation of the interface states, leading to the drift in device performance. For the APD, the drift is manifested as the increase in dark current or short failure. For the IC, the drift shows up as the shift in the threshold voltage.

Table III. Hot carrier injection of APD and its comparison with IC failure mechanism.

	APD	IC
Degradation pattern	Increase in dark current or short-circuit failure	Shift in the threshold voltage of CMOS transistor
Physical mechanism	Hot hole generation by the high electric field in the depletion layer and injection into the passivation dielectric	Hot carrier generation by the high lateral electric field in the source/drain channel and injection into the gate dielectric or into the transistor substrate
Aging method	Reverse bias, typically negative stress current of 100μA at 60-200°C.	DC stress involving the gate voltage and drain voltage at elevated temperature such as 150°C.

Based on the APD reliability model, it is predicted that highly reliable 10G/25G mesa-type APD devices may be feasible with the suppression of the weak links such as dielectric breakdown, mobile ion surface migration and hot carrier injection. The elimination of the weak links would be helpful to maintain stable surface/interface states and reduce the surface leakage current, resulting in low dark current for the long-term reliability performance.

4. Conclusion

We developed a predictive reliability model to account for the degradation behavior of 10G/25G mesa-type APD. For the mesa-type structure, surface dark current became dominant. We discussed the components of surface dark current in terms of dielectric breakdown, mobile ion migration and hot carrier injection. We also compared the degradation mechanisms of the APD degradation with those observed in the IC devices. The model predicted that highly reliable mesa-type APD were achievable with the suppression of weak links at the surface/interface states.

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